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Migrating LAN91C94 Designs to the LAN91C96

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The LAN91C96 is the new-generation 10 Mb/s SMSC Ethernet controller and includes support for IEEE 802.3 Full Duplex (FD) and Flow Control (FC). The LAN91C96 is pin compatible with the LAN91C94 and is intended as a direct replacement of the LAN91C94. The LAN91C96 also supports Magic Packet and the appropriate associated Power States. The controller also includes a real time counter for Early Receives for super-enhanced throughput. The LAN91C96 powers up in an LAN91C94 functionally equivalent state. All new features remain disabled until enabled by the software. The chip ID is also the same for the two with the exception of the Rev ID range.

The LAN91C96 adds the Configuration and Status Register (CSR) power down bit and, otherwise, supports the same version of the PCMCIA Configuration Option and Status Registers as the LAN91C94 to allow software driver compatibility between the two controllers. The CSR power down bit powers up clear (0) keeping the LAN91C96 compatible with the LAN91C94. Much like the LAN91C94, the LAN91C96 allows the PCMCIA Configuration and Status registers to be accessed via memory access; however, it also allows these registers to be accessed via I/O Bank 4.

The LAN91C96 is pin compatible with the LAN91C94 in both ISA and PCMCIA modes. With the two available in the same physical package, the LAN91C96 can be used as a drop-in replacement for the LAN91C94 in most applications.

The LAN91C96 also supports a subset to the Motorola 68000 microprocessor interface. The interface can be enabled when the chip is powered up in ISA mode. Enabling this mode changes the pin function for some of the pins.

The LAN91C96 provides 2Kbytes of additional RAM beyond the 4Kbytes of the LAN91C94. The additional memory helps to improve support for the Full duplex environment. It also helps with modern operating systems which introduce longer latencies in servicing controller requests. The chip's Memory Management Unit (MMU) manages the additional memory transparently and does not require any modifications to the software drivers.

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The following itemizes the differences between the two controllers:

ISA or PCMCIA PIN ASSIGNMENT DIFFERENCES

None

MOTOROLA 68000 MODE PIN ASSIGNMENT

The mode is supported in the LAN91C96 only. The following pins functions are changed:

- nIORD becomes data strobe (DS, LDS, or UDS)
- nIOWR becomes read or write select (R/nW)
- nAEN becomes address strobe (nAS)
- INT2 becomes DTACK or DTACK0 (symbol 'T' signifies the Data 'Transfer' part only of the Data Size and Transfer Acknowledge signal)
- INT3 becomes DTACK or DTACK1

The following signals must be pulled up or down as stated:

- LAN91C96 Address line 0 tied low (Only 16 bit data interface permitted)
- LAN91C96 nSBHE input tied low
- All DTACK/INTx must have a 1KΩ to 10KΩ pull-up to keep the line high while the drivers are tri-stated

The data upper and lower bytes should be swapped also to accommodate the big and little endian difference. The controller enters the Motorola mode if the nIORD and nIOWR are asserted simultaneously following the release of the reset. Once the two are asserted together, the first access to the controller must be a write. The mode is exited via a hard reset.

CHANGED REGISTERS

M (Memory Size Multiplier)

Lower byte of the Memory Information Register [Bank 0, Offset 8] reads back 18H to indicate the internal RAM size of 6144 bytes.

Auto TX Start Register

The upper byte [Bank 2, Offset 1] of the -Bank 2, Offset 0- MMU Command Register specifies the number of bytes (in multiples of 16) for the Early Transmit to begin transmitting the associated transmit buffer queued in the Transmit FIFO. The counter allows Early Transmit optimization to avoid TX underruns. Notice that the AutoTx and ETEN bits in the Pointer Register have to be set(1) for this register to be utilized.

Revision Register

The Revision ID reads '6' or higher for the LAN91C96 (same Device ID).

NEW REGISTERS (ACCESS MECHANISM)

The PCMCIA configuration Option and Status Registers can now be accessed via I/O Bank 4.

CHANGED BITS

Some of the formerly unused bits have been assigned new functions. These bits include Pwrdwn, FDSE, ETEN-TYPE, TXP_EN, WAKEUP, WAKEUP_EN, Command, CNTRL_PKT, AutoTx, and TX IDLE INT as described below:

Pwrdwn

Bit 2 of the Configuration and Status Register. In PCMCIA mode, when set (1), the bit puts the controller into a low power state. The bit powers up clear (0).

FDSE

Bit 15 of the Transmit Control Register [Bank 0, Offset 0], configures the LAN91C96 for full duplex switched Ethernet. When set (1), the LAN91C96 transmit and receive processes are fully independent. The controller transmission process does not defer to in-coming network traffic while in this mode. There are no back-offs also as no collisions can occur. Notice that the legacy FDUPLX bit still exists in the Transmit Control Register to support traditional loop-back testing. The FDSE defaults clear (0) at power up.

ETEN-TYPE

Bit 14 of the Transmit Control Register [Bank 0, Offset 0], allows to select the Early Transmit underrun detection type. When ETEN-TYPE is clear (0), ETEN bit set high (1) in the Pointer Register enables Early Transmit underrun function as implemented in LAN91C94. I.e. “The Early Transmit function allows the CPU to enqueue the first transmit packet before it is fully loaded in packet memory. The loading operation proceeds in parallel with the transmission - and in the case that the transmitter gets ahead of the CPU, the LAN91C96 prevents the transmission of erroneous data by forcing an Underrun condition. Underruns are triggered by starving the transmit DMA if the LAN91C96 detects that the DMA TX address exceeds the pointer address.”

With ETEN-TYPE set (1), ETEN bit set high (1) in the Pointer Register means: “For underrun detection purposes the RAM logical address and packet numbers of the packet being loaded are compared against the logical address and packet numbers of the packet being transmitted. If the packet numbers match and the logical address of the packet being transmitted exceeds the address being loaded, the LAN91C96 prevents the transmission of erroneous data by forcing an Underrun condition. Underruns are triggered by starving the transmit DMA if the LAN91C96 detects that the DMA TX address exceeds the pointer address.”

TXP_EN

Bit 3 of the Transmit Control Register [Bank 0, Offset 0], should remain clear (0). When the bit is set, it does not perform the intended function. The LAN91C96 does not pause transmission for a received Flow Control packet while in full duplex mode..

When the TXP EN bit set (1), the LAN91C96 receive state machine will not pause for a valid received flow control packet The flow control logic swaps the upper and lower byte of the Flow Control Header thus causing a mismatch condition.. For example, a packet with Type/Length 0888 and MAC Control Opcode of 0100 is detected by the flow control logic as having a Type/Length 8808 and MAC Control Opcode of 0001.The LAN91C96 will not detect a valid flow control packet and will not pause transmission. Therefore, the TXP_EN (Bit 3 of the TCR) should be cleared (0).

WAKEUP

Bit 8 of the Ethernet Protocol Handler (EPH) Status Register [Bank 0, Offset 2] indicates if a Magic Packet with the node's own Individual Address repetitions has been received. Notice that the scanning is performed only when the chip is in the appropriate low power mode. Defaults low (0).

WAKEUP_EN

Bit 12 of the Control Register [Bank 1, Offset C] to make the controller enter the appropriate power down state and start scanning the network for Magic Packets. Defaults disabled (0).

Command

Bit 4 of the MMU Command Register [Bank 2, Offset 0] to add additional commands. One command '0111' (7) is added to remove a non-flow control packet from the top of the Transmit FIFO. The command is used if regular transmit packets have been queued and a Flow Control packet needs to be put in the front of the transmit queue. Notice that this command must only be issued when the transmitter is idle.

CNTRL_PKT

Bit 7 of the Packet Number Register [Bank 2, Offset 2] allows the override of any pause time incurred due to a received Flow Control packet to transmit a FC packet immediately. Notice that setting (1) CNTRL_PKT will override any pause time due to the received FC only; setting (1) the bit will not override the CSMA/CD deferral in half duplex mode.

AutoTx

Bit 3 of the Pointer Register [Bank 2, Offset 6] enables the transmit state machine to automatically start transmitting (w/o host intervention) as soon as the number of bytes copied in the queued TX FIFO matches or exceeds the byte count indicated by the Auto TX Start Register. The Auto TX Start Register must contain a non-zero value for the AutoTx to function. Notice that the chip Early Transmit function (ETEN bit) must be enabled with RCV bit clear(0) for this feature to be used.

TX IDLE INT

Bit 7 of the Interrupt Status Register [Bank 2, Offset C] (and Bit 7 of the Interrupt Mask Register [Bank 2, Offset D]) is set (1) when the transmit state machine is not active. The interrupt is unmasked (or polled) under conditions that an FC packet needs to be transmitted while the TX FIFO is not empty. The interrupt allows a graceful and efficient wait for current transmit activity to end before attempting any MMU commands for FC packet queuing.

EXISTING BIT FUNCTIONALITY DIFFERENCES

RX_OVRN BIT IN EPH STATUS REGISTER

Definition: The RX_OVRN bit of the EPH Status register is set high (1) when a memory allocation within the RAM buffer fails upon receipt of a frame. As a result of the receive allocation failure, FIFO entries for the current frame are discarded. The receiver remains enabled and will receive subsequent frames if memory is available. This is the normal action the 9000 Family of Ethernet Controllers should take.

LAN91C94 Implementation:

The RX_OVRN bit of the EPH Status register functions as defined by the specification.

LAN91C96 Implementation:

For the LAN91C96, the RX_OVRN bit of the EPH Status register does not get set (1) when a memory allocation fails. All other functionality relating to the receiver overrunning is the same.

This is normally not a problem since no SMSC supported drivers check this bit. The RX_OVRN bit of the Interrupt Status Register serves the same purpose as the RX_OVRN bit of the EPH Status Register and should be used as an indicator of a receiver overrun.

INTERFACE SIGNAL CHARACTERISTICS AND BEHAVIOR

SRESET BIT IN ETHERNET CONFIGURATION OPTION REGISTER (ECOR) EFFECT ON THE nIREQ/READY SIGNAL

In PCMCIA mode, the nIREQ/READY signal performs the ready function during power up (remains low until the device is ready to be accessed) after which, it behaves as an active low interrupt request. SRESET (Bit 7 of the ECOR) when set (1), performs a soft reset function (clears the Ethernet registers associated with the Ethernet function, except for bit 7 itself and triggers an EEPROM read). When SRESET is set, the nIREQ/READY signal is not effected.

LAN91C94 Implementation:

SRESET (Bit 7 of the ECOR) is fully supported by the LAN91C94.

LAN91C96 Implementation:

For the LAN91C96, the SRESET, when set (1), asserts an active low ready function on the nIREQ/READY signal until the device is ready to be accessed. This low signal on the PCMCIA interface is interpreted as an interrupt request. As a result, when SRESET is set, the nIREQ/READY signal is effected which is different with respect to the LAN91C94 implementation.

It should be noted that commercially available system I/O configuration and device driver software do not utilize this bit. The SOFT RST bit in the Receive Control Register provides an effective means of resetting the LAN91C96. The LAN9000 driver is the only software module that should assert this bit. If the assertion of the nIREQ/READY signal is not a recommended event for the particular environment the driver/card is designed for, the SRESET bit should not be asserted.