National Semiconductor

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NS32FX210 Facsimile/Data Modem Analog Front End (AFE)

General Description

The NS32FX210 is a highly integrated A/D and D/A Converters with Filtering device optimized for FAX and data modem analog front end applications. Using advanced switched capacitor techniques, AFE combines receive bandpass and transmit lowpass channel filters with a companding PCM encoder and decoder. The device employs a conventional serial PCM interface capable of being clocked at 1.536 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active Data Access Arrangement (DAA) circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable AFE to interface to the DAA circuit, six programmable latches are included; each may be configured as either an input or an output.

Features

- Transmit and receive PCM channel filters
- μ-law companding encoder and decoder
- Transmit power amplifier drives 300Ω
- 1.536 MHz serial PCM data
- Programmable Functions:
  - — Receive gain: 25.4 dB range, 0.1 dB steps
  - — Transmit gain: 25.4 dB range, 0.1 dB steps
  - — Hybrid balance cancellation filter
  - — 6 interface latches
  - — Analog loopback
  - — Digital loopback
- Direct interface to single secondary winding line transformer
- Standard serial control interface
- 80 mW operating power (typ)
- 1.5 mW standby power (typ)
- TTL and CMOS compatible digital interfaces

Block Diagram

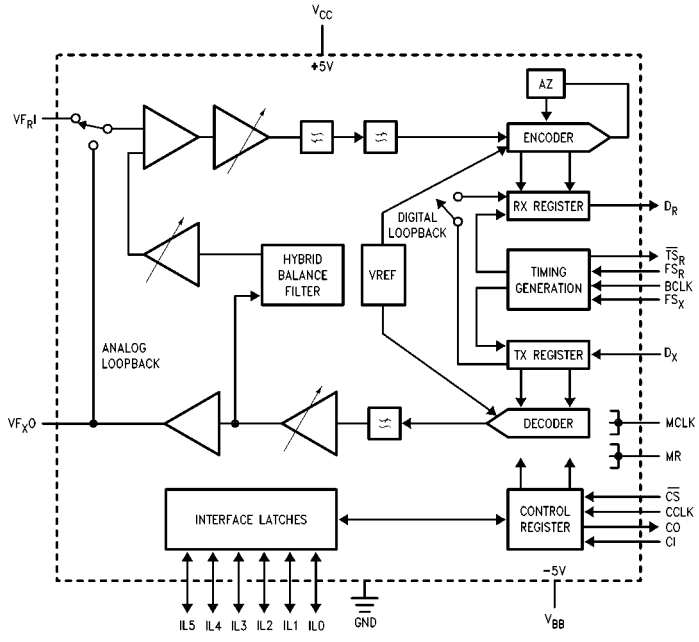

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FIGURE 1

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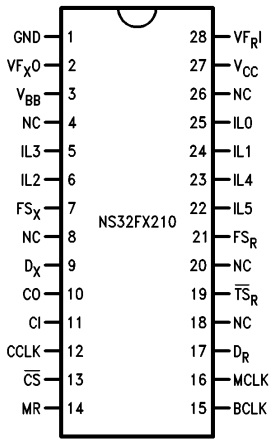
Connection Diagrams



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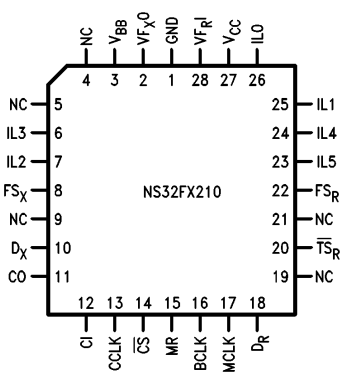
Order Number NS32FX210J
See NS Package Number J28A



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Order Number NS32FX210V
See NS Package Number V28A

Pin Descriptions

Pin	Description
V_{CC}	+5V ±5% power supply.
V_{BB}	−5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS_R	Receive Frame Sync Input. Normally a pulse or squarewave with an 8 kHz or 9.6 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device.
FS_X	Transmit Frame Sync Input. Normally a pulse or squarewave with an 8 kHz or 9.6 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device.
BCLK	Bit clock input used to shift PCM data into and out of the D_X and D_R pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 1.536 MHz and synchronous with BCLK.
VF_RI	The Receive analog high-impedance input. Voice frequency signals present on this input are encoded as a μ-law PCM bit stream and shifted out on the D_R pin.
VF_XO	The Transmit analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the D_X pin is decoded and appears at this output as voice frequency signals.
D_R	This Receive Data TRI-STATE® output remains in the high impedance state except during the receive time slot during which the receive PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS}_R$	Normally this open-drain output is floating in a high impedance state. It pulls low when a time-slot is active on the D_R output.
D_X	This transmit data input is inactive except during the transmit time slot when the transmit PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock Input. This clock shifts serial control information into or out from CI and CO when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI	Serial control data is shifted into the AFE via this pin when $\overline{CS}$ is low. It can be connected to CO if required.
CO	Serial control data is read out of AFE via this pin when $\overline{CS}$ is low and a read has been requested in Byte 1 of the control instruction. It can be connected to CI if required.
$\overline{CS}$	Chip Select Input. When this pin is low, control information can be written to or read from AFE via the CI and CO pin.
IL5–IL0	Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to the AFE, while $\overline{CS}$ is low, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
MR	This logic input must be pulled low for normal operation of the AFE. When pulled momentarily high (at least 1 μs), all programmable registers in the device are reset to the states specified under ''Power-On Initialization''.
NC	No Connection. Do not connect to this pin. Do not route traces through this pin.

Functional Description

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the AFE and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed to OFF (00000000), the hybrid balance circuit is turned off and the power amp is disabled. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the DAA interface pins in a high impedance state. Other initial states in the Control Register are indicated in Section 2.0.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low. If not used, MR should be hardwired to ground.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the ''P'' bit set to ''1'' as indicated in Table I. It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D_R output is in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintainng the ability to monitor and control the DAA.

RECEIVE FILTER AND ENCODER

The receive section input, VF_RI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are necessary to set the gain. Following this circuit is a programmable gain amplifier which is controlled by the contents of the Receive Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard μ255 coding law. A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the Receive time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Receive Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_R during the time slot on eight rising edges of BCLK.

DECODER AND TRANSMIT FILTER

PCM data is shifted into the Decoder's Transmit PCM Register via the D_X pin during the time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with μ255 law decoding characteristic. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz or 9.6 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Transmit Gain Register, is included, and finally a Power Amplifier capable of driving a 300Ω load to $\pm$3.5V, a 600Ω load to $\pm$3.8V or a 15 kΩ load to $\pm$4.0V at peak overload.

A decode cycle begins immediately after the transmit time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (½ frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_R and FS_X frame sync inputs determine the beginning of the 8-bit receive and transmit time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW.

Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). In Non-delayed Data Timing mode, time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data Timing mode in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot.

Receive and Transmit frames and time-slots may be skewed from each other by any number of BCLK cycles. During each Receive time-slot, the D_R output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_R$ also pulls low for the first 7½ bit times of the time-slot. Serial PCM data is shifted into the D_X input during each Transmit time-slot on the falling edges of BCLK.

Functional Description (Continued)

SERIAL CONTROL PORT

Control information and data are written into or read-back from the AFE via the serial control port consisting of the control clock CCLK, the serial data input, CI, and output, CO, and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed in Table I, with the exception of a single byte power-up/down command. The byte 1 bits are used as follows: bit 7 specifies power up or power down; bits 6, 5, 4, and 3 specify the register address; bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into the AFE, CCLK must be pulsed 8 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i.e., it is not mandatory for $\overline{CS}$ to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ should be set high when no data transfers are in progress.

To readback Interface Latch data or status information from the AFE, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in Table I. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO pin is in the high-impedance TRI-STATE, enabling the CO pins of many devices to be bussed together.

Programmable Functions

1.0 POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instuctions listed in Table I into the AFE with the ''P'' bit set to ''0'' for power-up or ''1'' for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the ''P'' bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output, D_R, will remain in the high impedance state until the second FS_R pulse after power-up.

2.0 CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction for the Control Register is as shown in Table I. The second byte has the bit functions shown in Table II.

TABLE I. Programmable Register Instructions

Function	Byte 1 (Note 1)								Byte 2 (Note 1)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table II							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table II							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table V							
Read Interface Latch Regiser	P	0	0	0	1	1	1	X	See Table V							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table IV							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table IV							
Write Transmit Gain Register	P	0	1	0	0	0	1	X	See Table VIII							
Read Transmit Gain Register	P	0	1	0	0	1	1	X	See Table VIII							
Write Receive Gain Register	P	0	1	0	1	0	1	X	See Table VII							
Read Receive Gain Register	P	0	1	0	1	1	1	X	See Table VII							
Write Transmit PCM Enable/Disable	P	1	0	0	1	0	1	X	(Note 4)							
Read Transmit PCM Enable/Disable	P	1	0	0	1	1	1	X	(Note 4)							
Write Receive PCM Enable/Disable	P	1	0	1	0	0	1	X	(Note 4)							
Read Receive PCM Enable/Disable	P	1	0	1	0	1	1	X	(Note 4)							

Note 1: Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI or CO pin. X = don't care.

Note 2: ''P'' is the power-up/down control bit, see ''Power-Up/Down Control'' section. (''0'' = Power Up, ''1'' = Power Down)

Note 3: Three additional registers are provided for the Hybrid Balance Fitler, see Section 8.0. Other register address codes are invalid and should not be used.

Note 4: Enable code = 1000 0000, Disable Code = 0000 0000

Programmable Functions (Continued)

TABLE II. Control Register Byte 2 Functions

Bit Number								Function
7	6	5	4	3	2	1	0	
0	1	0	0					(Note 1)
				0				Delayed Data Timing
				1				Non-Delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization (Bits 7, 6, 5, 4 = 1, 0, 0, 0).

Note 1: Bits 7, 6, 5, 4 must always be programmed to 0, 1, 0, 0.

2.1 Analog Loopback

Analog Loopback mode is entered by setting the ''AL'' and ''DL'' bits in the Control Register as shown in Table II. In the analog loopback mode, the Receive input VF_RI is isolated from the input pin and internally connected to the VF_XO output, forming a loop from the Transmit PCM Register back to the Receive PCM Register. The VF_XO pin remains active, and the programmed settings of the Receive and Transmit gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop. Hybrid balance must be disabled for meaningful analog loopback function.

2.2 Digital Loopback

Digital Loopback mode is entered by setting the ''AL'' and ''DL'' bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Transmit PCM Register to be read back from that register in the Receive time-slot at D_R. In digital loopback, the decoder will remain functional and output a signal at VF_XO. If this is undesirable, the transmit output can be turned off by programming the transmit gain register to all zeros.

TABLE III. Coding Law Convention

	μ255 Law							
	MSB							LSB
V_{IN} = +Full Scale	1	0	0	0	0	0	0	0
V_{IN} = 0V	1	1	1	1	1	1	1	1
	0	1	1	1	1	1	1	1
V_{IN} = −Full Scale	0	0	0	0	0	0	0	0

Note 1: The MSB is always the first PCM bit shifted in or out of the AFE.

3.0 INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV. For minimum power dissipation, unconnected latch pins should be programmed as outputs.

Bits L_5–L_0 must be set by writing the specified instruction to the LDR with the L bits in the second byte set as follows:

TABLE IV. Byte 2 Functions of Latch Direction Register

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
L_0	L_1	L_2	L_3	L_4	L_5	X	X

L_n Bit	IL Direction
0	Input
1	Output

X = Don't Care

4.0 INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the ring detect output of a DAA. All bits of the ILR, i.e., sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first, followed immediately by the Latch Direction Register.

TABLE V. Interface Latch Data Bit Order

Bit Number							
7	6	5	4	3	2	1	0
D_0	D_1	D_2	D_3	D_4	D_5	X	X

Programmable Functions (Continued)

5.0 RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VI. This corresponds to a range of 0 dBm0 levels at VF_RI between 1.619 V_{rms} and 0.087 V_{rms} (equivalent to +6.4 dBm to −19.0 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in V_{rms}, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.08595)$$

and convert to the binary equivalent. Some examples are given in Table VI.

TABLE VI. Byte 2 of Receive Gain Instruction

Bit Number								0 dBm0 Test Level (V_{rms})
7	6	5	4	3	2	1	0	at VF_RI
0	0	0	0	0	0	0	0	No Output
0	0	0	0	0	0	0	1	0.087
0	0	0	0	0	0	1	0	0.088
				—				—
1	1	1	1	1	1	1	0	1.600
1	1	1	1	1	1	1	1	1.619

6.0 TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VII. Note the following restrictions on output drive capability:

a. 0 dBm0 levels ≤ 1.96 V_{rms} at VF_XO may be driven into a load of ≥ 15 kΩ to GND; transmit gain set to 0 dB

b. 0 dBm0 levels ≤ 1.85 V_{rms} at VF_XO may be driven into a load of ≥ 600Ω to GND; transmit gain set to −0.5 dB

c. 0 dBm0 levels ≤ 1.71 V_{rms} at VF_XO may be driven into a load of ≥ 300Ω to GND; transmit gain set to −1.2 dB

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in V_{rms}, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043)$$

and convert to the binary equivalent. Some examples are given in Table VII.

TABLE VII. Byte 2 of Transmit Instruction

Bit Number								0 dBm0 Test Level (V_{rms})
7	6	5	4	3	2	1	0	at VF_XO
0	0	0	0	0	0	0	0	No Output (Low Z to GND)
0	0	0	0	0	0	0	1	0.105
0	0	0	0	0	0	1	0	0.107
				—				—
1	1	1	1	1	1	1	0	1.941
1	1	1	1	1	1	1	1	1.964

7.0 PCM INTERFACE ENABLE/DISABLE

When power is first applied to the device pins, the PCM interface is disabled. To enable the PCM interface, both transmit and receive PCM Enable/Disable registers must be written with the enable code (1000 0000). See Table I.

8.0 HYBRID BALANCE FILTER

The Hybrid Balance Filter on the AFE is a programmable filter consisting of a second-order section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the receive input relative to the transmit output signal. The 2nd order section is intended mainly to balance low frequency signals across a transformer DAA, and the first order section to balance midrange to higher audio frequency signals.

As a 2nd order section, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring Hybal1, matching the phase of the hybrid at low to mid-band frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The 2nd order mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low-frequency pole and zero. In this mode, the pole/zero frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic DAA and is also helpful with a transformer DAA in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less. Independent placement of the pole and zero location is provided.

Figure 2 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_RI are a function of the termination impedance Z_T, the line transformer and the impedance of the 2W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_XO to VF_RI is:

$$H(w) = Z_L'/(Z_T + Z_L') \quad (1)$$

8.1 Programming the Filter

When power is first applied, the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2W input return loss specifications, which are normally measured against a fixed test impedance (600Ω or 900Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance. This test impedance is Z_L in *Figure 2*. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, D_X, to the PCM digital output, D_R, either by digital test signal analysis or by conversion back to analog by another AFE device.

Programmable Functions (Continued)

Three registers must be programmed in the AFE to fully configure the Hybrid Balance Filter as follows:

Register 1: select/de-select Hybrid Balance Filter;
invert/non-invert cancellation signal;
select/de-select Hybal2 filter section;
attenuator setting.

Register 2: select/de-select Hybal1 filter;
set Hybal1 to 2nd order or 1st order;
pole and zero frequency selection.

Register 3: program pole frequency in Hybal2 filter;
program zero frequency in Hybal2 filter.

Standard filter design techniques may be used to model the echo path (see Equation 1) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter designed to replicate it.

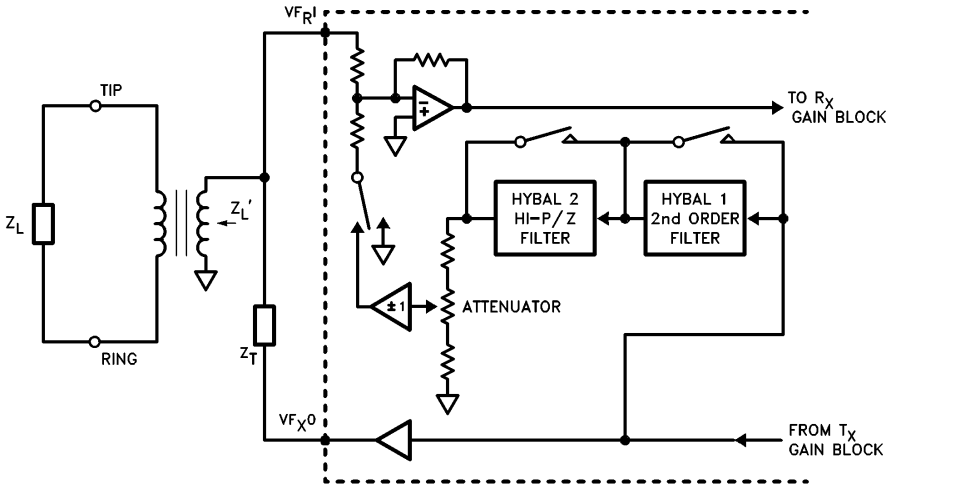

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FIGURE 2. Simplified Diagram of Hybrid Balance Circuit

Applications Information

Figure 3 shows a typical application of the AFE together with a transformer-based DAA. One of the IL latches is configured as an output to control the relay driver on the DAA while another is an input for the ring detect signal.

POWER SUPPLIES

While the pins of the AFE device are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, extra long pins on the connector should be used for ground and V_{BB}. In addition, a Schottky diode should be connected between V_{BB} and ground.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the device GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common device ground point to V_{CC} and V_{BB} as close to the device pins as possible. V_{CC} and V_{BB} should also be decoupled with Low Effective Series Resistance Capacitors of at least 10 μF located near the card edge connector.

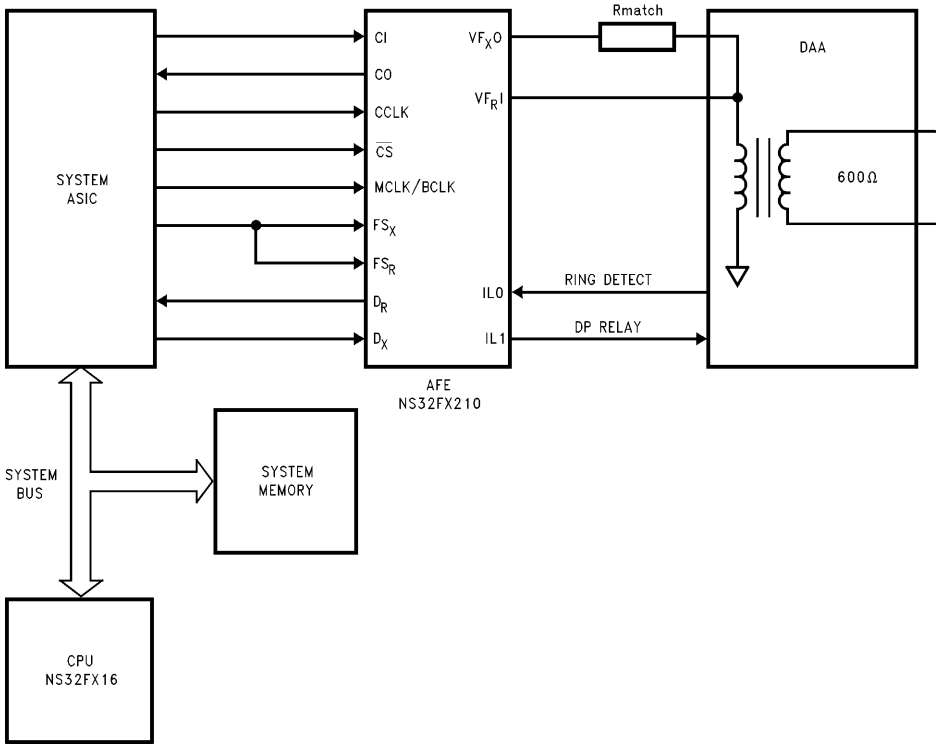

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FIGURE 3. Stand-Alone FAX Application

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at VF_RI	V_{CC} + 0.5V to V_{BB} − 0.5V
Voltage at any Digital Input	V_{CC} + 0.5V to GND − 0.5V
Storage Temperature Range	−65°C to +150°C
V_{BB} to GND	−7V
Current at VF_XO	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs (DC Meas.)*			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs (DC Meas.)*	**2.0**			V
V_{OL}	Output Low Voltage	D_R, $\overline{TS}_R$ and CO, I_L = 3.2 mA, All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_R and CO, I_L = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_R$), I_L = −1 mA All Digital Outputs, I_L = −100 μA	**2.4** V_{CC} −0.5			V V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	μA
I_{IH}	Input High Current	Any Digital Input Except MR, V_{IH} < V_{IN} < V_{CC}	**−10**		**10**	μA
		MR Only	**−10**		**100**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_R and CO IL5–IL0 When Selected as Inputs GND < V_{OUT} < V_{CC}	**−10**		**10**	μA
ANALOG INTERFACES						
I_{VFRI}	Input Current, VF_RI	−3.3V < VF_RI < 3.3V	**−10.0**		**10.0**	μA
R_{VFRI}	Input Resistance	−3.3V < VF_RI < 3.3V	**390**	620		kΩ
VOS_R	Input Offset Voltage Applied at VF_RI	Receive Gain = 0 dB Receive Gain = 25.4 dB			200 10	mV mV
RL_{VFXO}	Load Resistance	Transmit Gain = 0 dB Transmit Gain = −0.5 dB Transmit Gain = −1.2 dB	15k 500 **300**			Ω
CL_{VFXO}	Load Capacitance	RL_{VFXO} ≥ 300Ω CL_{VFXO} from VF_XO to GND			**200**	pF
RO_{VFXO}	Output Resistance	Steady Zero PCM Code Applied to D_X		1.0	3.0	Ω
VOS_X	Output Offset Voltage at V_{FXO}	Alternating ± Zero PCM Code Applied to D_X, 0 dB Transmit Gain	**−200**		**200**	mV

*__Note:__ See definitions and timing conventions section.

Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	CCLK, CI, CO, = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled		0.1	**0.6**	mA
$I_{BB}0$	Power Down Current	As Above		−0.1	**−0.3**	mA
$I_{CC}1$	Power Up Current	CCLK, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load		8.0	**11.0**	mA
$I_{BB}1$	Power Up Current	As Above		−8.0	**−11.0**	mA
$I_{CC}2$	Power Down Current	Power Amp Enabled		2.0	**3.0**	mA
$I_{BB}2$	Power Down Current	Power Amp Enabled		−2.0	**−3.0**	mA

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK TIMING						
f_{MCLK}	Frequency of MCLK			1536		kHz
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBM}	HOLD Time, BCLK LOW to MCLK HIGH		**50**			ns
t_{WFL}	Period of F_{SR} or F_{SX} Low	Measured from V_{IL} to V_{IL}	1			MCLK Period
PCM INTERFACE TIMING						
f_{BCLK}	Frequency of BCLK	May Vary from 64 kHz to 4096 kHz in 8 kHz Increments	**64**		**4096**	kHz
t_{WBH}	Period of BCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WBL}	Period of BCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RB}	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FB}	Fall Time of BCLK	Measured from V_{IH} to V_L			30	ns

Timing Specifications (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PCM INTERFACE TIMING (Continued)						
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		**30**			ns
t_{SFB}	Setup Time, $FS_{R/X}$ High to BCLK Low		**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns
t_{DBZ}	Delay Time, BCLK Low to D_R Disabled if FS_R Low, FS_R Low to D_R Disabled if 8th BCLK Low, or BCLK High to D_R Disabled if FS_R High		**15**		**80**	ns
t_{DBT}	Delay Time, BCLK High to $\overline{TS}_R$ Low if FS_R High, or FS_R High to $\overline{TS}_R$ Low if BCLK High	Load = 100 pF Plus 2 LSTTL Loads			60	ns
t_{ZBT}	TRI-STATE Time, BCLK Low to $\overline{TS}_R$ High if FS_R Low, FS_R Low to $\overline{TS}_R$ High if 8th BCLK Low, or BCLK High to $\overline{TS}_R$ High if FS_R High		15		60	ns
t_{DFD}	Delay Time, $FS_{X/R}$ High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only			**80**	ns
t_{SDB}	Setup Time, D_X Valid to BCLK Low		**30**			ns
t_{HBD}	Hold Time, BCLK Low to D_X Invalid		**20**			ns
SERIAL CONTROL PORT TIMING						
f_{CCLK}	Frequency of CCLK				**2048**	kHz
t_{WCH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**160**			ns
t_{WCL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	**160**			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low	CCLK1	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High	CCLK8	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low		**60**			ns

Timing Specifications (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL CONTROL PORT TIMING (Continued)						
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High		80			ns
t_{SDC}	Setup Time, CI Data In to CCLK Low		**80**			ns
t_{HCD}	Hold Time, CCLK Low to CI Invalid		50			ns
t_{DCD}	Delay Time, CCLK High to CO Data Out Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO Valid	Applies Only if Separate $\overline{CS}$ used for Byte 2			**80**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or 9th CCLK High to CO High Impedance	Applies to Earlier of $\overline{CS}$ High or 9th CCLK High	15		80	ns
INTERFACE LATCH TIMING						
t_{SLC}	Setup Time, IL to CCLK 8 of Byte 1	Interface Latch Inputs Only	**100**			ns
t_{HCL}	Hold Time, IL Valid from 8th CCLK Low (Byte 1)		50			ns
t_{DCL}	Delay Time CCLK 8 of Byte 2 to IL	Interface Latch Outputs Only $C_L = 50$ pF			200	ns
MASTER RESET PIN						
t_{WMR}	Duration of Master Reset High		1			μs

Timing Diagrams

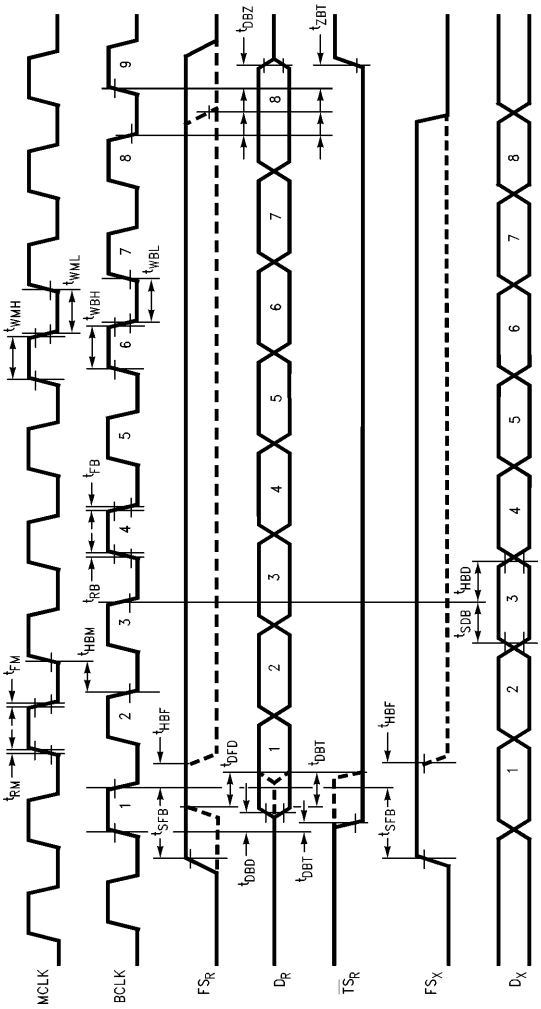


FIGURE 4. Non-Delayed Data Timing Mode

Timing Diagrams (Continued)

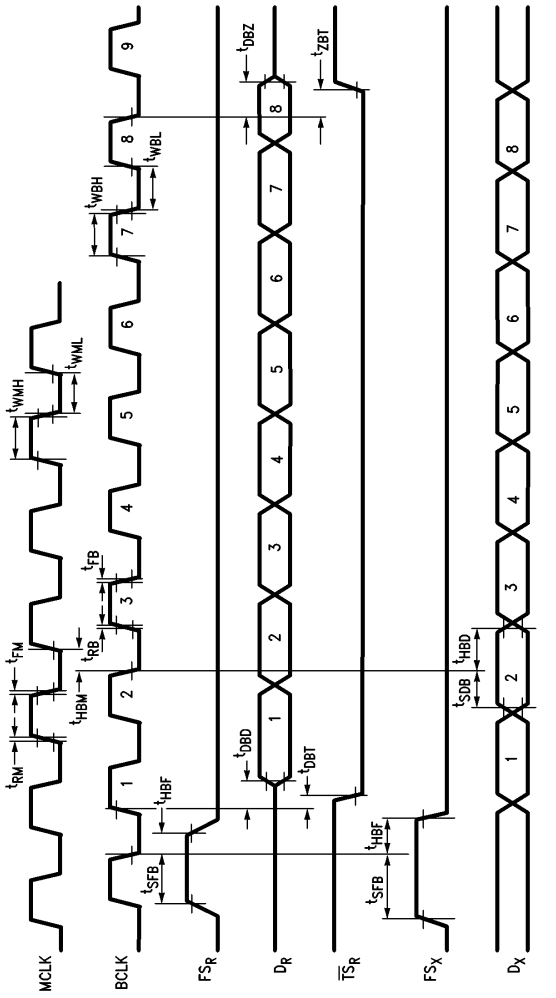


FIGURE 5. Delayed Data Timing Mode

Timing Diagrams (Continued)

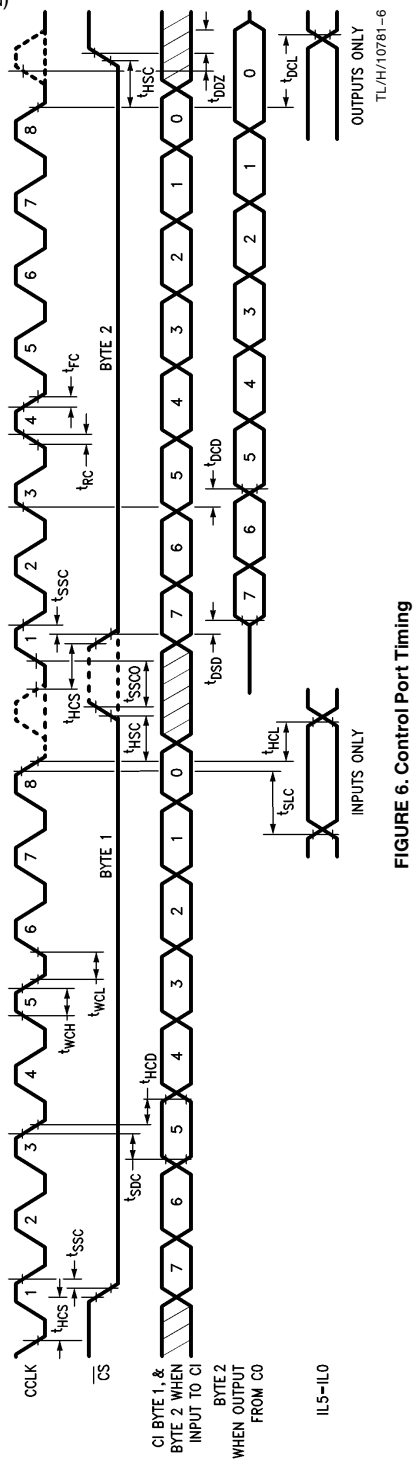


FIGURE 6. Control Port Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; FS_R and FS_X = 8 kHz or 9.6 kHz; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_RI = 0 dBm0, D_X = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	The Maximum 0 dBm0 Levels are: VF_RI VF_XO (15 kΩ Load)		 1.619 1.964		 Vrms Vrms
		The Minimum 0 dBm0 Levels are: VF_RI VF_XO (Any Load ≥ 300Ω) Overload Level is 3.17 dBm0		 87.0 105.0		 mVrms mVrms
G_{RA}	Receive Gain Absolute Accuracy	Receive Gain Programmed for Maximum 0 dBm0 Test Level. (All 1's in gain register) Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at D_R T_A = 25°C	**−0.15**		**0.15**	dB
G_{RAG}	Receive Gain Variation with Programmed Gain	Measure Receive Gain Over the Range from Maximum to Minimum Calculate the Deviation from the Programmed Gain Relative to G_{RA}, i.e., $G_{RAG} = G_{actual} - G_{prog} - G_{RA}$ T_A = 25°C, $V_{CC} = -5V$, $V_{BB} = -5V$	**−0.1**		**0.1**	dB
G_{RAF}	Receive Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) Minimum Gain < G_R < Maximum Gain				
		f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		f ≥ 4600 Hz. Measure Response at Alias Frequency from 0 kHz to 4 kHz G_R = 0 dB, VF_R = 1.619 Vrms			−32	dB
		Relative to 1015.625 Hz				
		f = 62.5 Hz			**−24.9**	dB
		f = 203.125 Hz	**−1.7**		**−0.1**	dB
		f = 343.75 Hz	**−0.15**		**0.15**	dB
		f = 515.625 Hz	**−0.15**		**0.15**	dB
		f = 2140.625 Hz	**−0.15**		**0.15**	dB
		f = 3156.25 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
		Relative to 1062.5 Hz (Note 4)				
		f = 5250 Hz, Measure 2750 Hz			**−32**	dB
		f = 11750 Hz, Measure 3750 Hz			**−32**	dB
		f = 49750 Hz, Measure 1750 Hz			**−32**	dB
G_{RAT}	Receive Gain Variation with Temperature	Measured Relative to G_{RA}, $V_{CC} = 5V$, $V_{BB} = -5V$, Minimum Gain < G_R < Maximum Gain	−0.1		0.1	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; FS_R and FS_X = 8 kHz or 9.6 kHz; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_RI = 0 dBm0, D_X = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{RAL}	Receive Gain Variation with Signal Level	Sinusoidal Test Method Reference Level = 0 dBm0 VF_RI = −40 dBm0 to +3 dBm0 VF_RI = −50 dBm0 to −40 dBm0 VF_RI = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for Maximum 0 dBm0 Test Level (All 1's in Gain Register). Apply 0 dBm0 PCM Code to D_X. Measure VF_XO. T_A = 25°C	**−0.3**		**0.3**	dB
G_{XAG}	Transmit Gain Variation with Programmed Gain	Measure Transmit Gain Over the Range from Maximum to Minimum Setting. Calculate the Deviation from the Programmed Gain Relative to G_{XA}, i.e., $G_{XAG} = G_{actual} - G_{prog} - G_{XA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V	**−0.2**		**0.2**	dB
G_{XAT}	Transmit Gain Variation with Temperature	Measured Relative to G_{XA} V_{CC} = 5V, V_{BB} = −5V Minimum Gain < G_X < Maximum Gain	−0.1		0.1	dB
G_{XAF}	Transmit Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) G_X = 0 dB, D_X = 0 dBm0 Code, G_R = 0 dB (Note 4) f = 296.875 Hz f = 1875.00 Hz f = 2906.25 Hz f = 2984.375 Hz f = 3406.250 Hz f = 3984.375 Hz	 **−0.15** **−0.15** **−0.15** **−0.15** **−0.74** 		 **0.16** **0.41** **0.78** **0.82** **0.89** **−12.2**	 dB dB dB dB dB dB
G_{XAL}	Transmit Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0 D_X = −40 dBm0 to +3 dBm0 D_X = −50 dBm0 to −40 dBm0 D_X = −55 dBm0 to −50 dBm0 D_X = 3.1 dBm0 R_L = 600Ω, G_X = −0.5 dB R_L = 300Ω, G_X = −1.2 dB	 **−0.2** **−0.4** **−1.2** −0.2 **−0.2**		 **0.2** **0.4** **1.2** 0.2 **0.2**	 dB dB dB dB dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; FS_R and $FS_X = 8$ kHz or 9.6 kHz; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. f = 1015.625 Hz, $VF_RI = 0$ dBm0, $D_X = 0$ dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE						
N_{RC}	Receive Noise, C Message Weighted	(Note 1) All '1's in Gain Register		12	**15**	dBrnC0
N_{XC}	Transmit Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{XS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_RI = 0$ Vrms			−53	dBm0
$PPSR_R$	Positive Power Supply Rejection, Receive	$V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 kHz − 4 kHz (Note 2) f = 4 kHz − 50 kHz	**36** 30			dBC dBC
$NPSR_R$	Negative Power Supply Rejection, Receive	$V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 kHz − 4 kHz (Note 2) f = 4 kHz − 50 kHz	**36** 30			dBC dBC
$PPSR_X$	Positive Power Supply Rejection, Transmit	PCM Code Equals Positive Zero $V_{CC} = 5.0\ V_{DC} + 100$ mVrms Measure VF_XO f = 0 Hz–4000 Hz f = 4 kHz–25 kHz f = 25 kHz–50 kHz	 **36** 40 36			 dBC dB dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	PCM Code Equals Positive Zero $V_{BB} = -5.0\ V_{DC} + 100$ mVrms Measure VF_XO f = 0 Hz–4000 Hz f = 4 kHz–25 kHz f = 25 kHz–50 kHz	 **36** 40 36			 dBC dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_X 4600 Hz–7600 Hz 7600 Hz–8400 Hz 8400 Hz–50,000 Hz			 **−30** **−40** **−30**	 dB dB dB
DISTORTION						
STD_R STD_X	Signal to Total Distortion Receive or Transmit Half-Channel	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 = −45 dBm0	 **33** **36** **30** **25**			 dBC dBC dBC dBC
STD_{XL}	Signal to Total Distortion Transmit with Resistive Load	Sinusoidal Test Method Level = +3.1 dBm0 $R_L = 600\Omega$, $G_X = -0.5$ dB $R_L = 300\Omega$, $G_X = -1.2$ dB	 33 **33**			 dBC dBC

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; FS_R and FS_X = 8 kHz or 9.6 kHz; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_RI = 0 dBm0, D_X = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
SFD_R	Signal Frequency Distortion, Receive				**−46**	dB
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
IMD	Intermodulation Distortion	Receive or Transmit Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB

Note 1: Measured by grounded input at VF_RI.

Note 2: $PPSR_R$, $NPSR_R$, are measured with a −50 dBm0 activation signal applied to VF_RI.

Note 3: A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply:

a) All input signals are defined as: $V_{IL} = 0.4V$, $V_{IH} = 2.7V$, $t_X < 10$ ns, $t_F < 10$ ns.

b) t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}.

c) Delay Times are measured from the input signal Valid to the output signal Valid.

d) Setup Times are measured from the data input Valid to the clock input Invalid.

e) Hold Times are measured from the clock signal Valid to the data input Invalid.

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

Note 4: A multi-tone test technique is used.

Definitions and Timing Conventions

DEFINITIONS

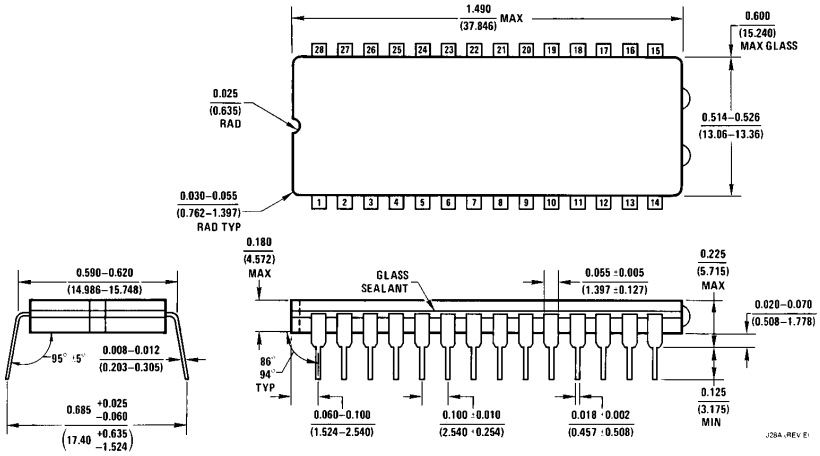
V_{IH}	V_{IH} is the D.C. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e., not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the D.C. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states. (i.e., above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply.

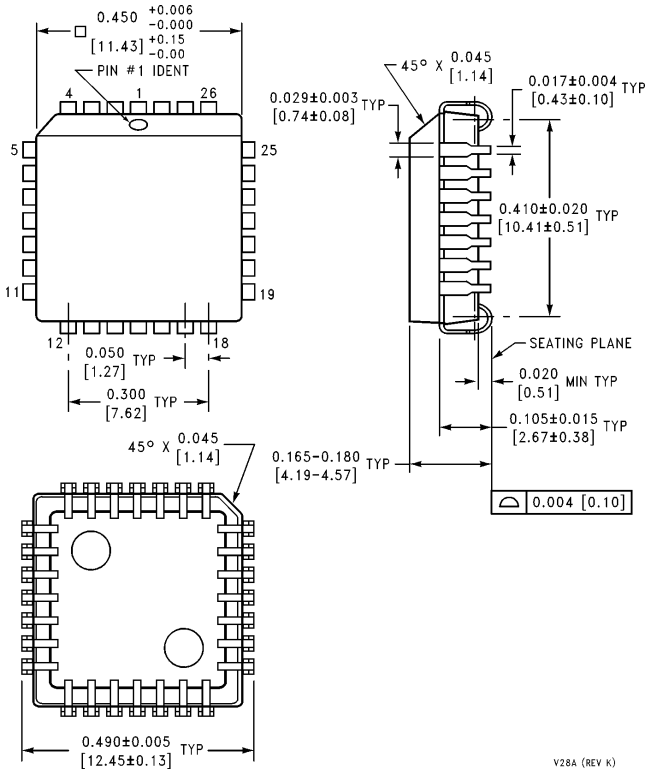
Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.
Period	The period of the clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as T_{Hwwxx}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as T_{Dxxyy}[IHIL], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

Physical Dimensions inches (millimeters)



Order Number NS32FX210J
NS Package Number J28A

Physical Dimensions inches (millimeters) (Continued)



Plastic Leaded Chip Carrier (V)
Order Number NS32FX210V
NS Package Number V28A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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