SILICON LABORATORIES

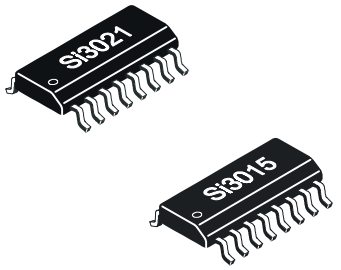
Si3044

3.3 V Enhanced Global Direct Access Arrangement

Features

Complete DAA includes the following:

- Line Voltage Monitor
- Loop Current Monitor
- 3.2 dBm Transmit/Receive Levels
- Parallel Handset Detection
- 7 µA On-Hook Line Monitor Current
- Overload Protection
- Programmable Line Interface
  - AC Termination
  - DC Termination
  - Ring Detect Threshold
  - Ringer Impedance
- Polarity Reversal Detection
- 84 dB Dynamic Range TX/RX
- Integrated Analog Front End (AFE) and 2- to 4-Wire Hybrid
- Integrated Ring Detector
- Caller ID Support
- Pulse Dialing Support
- Billing Tone Detection
- 3.3 V or 5 V Power Supply
- Direct Interface to DSPs
- Daisy-Chaining for Up to Eight Devices
- 3000 V Isolation
- Proprietary ISOcap™ Technology
- Pin Compatible with Si3034



Ordering Information

See page 67.

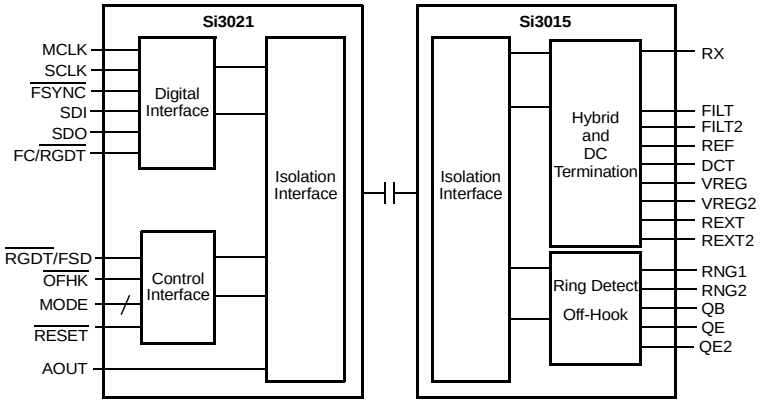
Applications

- V.90 Modems
- Set Top Boxes
- Internet Appliances
- Voice Mail Systems
- Fax Machines
- VOIP Systems

Description

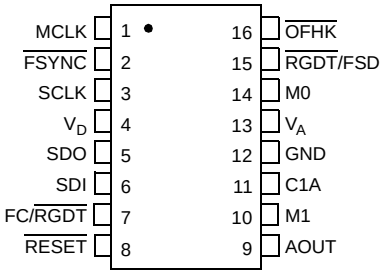
The Si3044 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. Available in two 16-pin small outline packages, it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3044 dramatically reduces the number of discrete components and cost required to achieve compliance with global regulatory requirements. The Si3044 interfaces directly to standard modem DSPs.

Functional Block Diagram

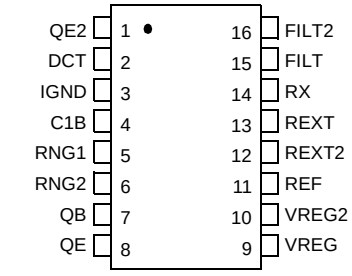


Pin Assignments

Si3021



Si3015



US Patent# 5,870,046
US Patent# 6,061,009
Other Patents Pending

TABLE OF CONTENTS

SILICON LABORATORIES

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Ambient Temperature	T_A	B-Grade	–40	25	85	°C
Si3021 Supply Voltage, Analog	V_A		4.75	5.0	5.25	V
Si3021 Supply Voltage, Digital[3]	V_D		3.0	3.3/5.0	5.25	V

Notes:

1. The Si3044 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si3021 and any Si3015 are used. See Figure 16 on page 15 for the typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, can operate from either 3.3 V or 5.0 V. The Si3021 supports interfacing to 3.3 V logic when operating from 3.3 V. This applies to both the serial port and the digital signals $\overline{\text{RGDT}}$/FSD, $\overline{\text{OFHK}}$, $\overline{\text{RESET}}$, M0, and M1.

Table 2. Loop Characteristics

(V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade and –40 to 85°C for B-Grade, See Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 1 DCT = 11 (CTR21)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 42 mA, ACT = 1 DCT = 11 (CTR21)	—	—	14.5	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ACT = 1 DCT = 11 (CTR21)	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ACT = 1 DCT = 11 (CTR21)	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 01 (Japan)	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 01 (Japan)	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 10 (FCC)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 10 (FCC)	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 15 mA, ACT = 0 DCT = 00 (Low Voltage)	—	—	5.2	V
On Hook Leakage Current[1]	I_{LK}	V_{TR} = –48V	—	—	7	µA
Operating Loop Current	I_{LP}	FCC / Japan Modes	13	—	120	mA
Operating Loop Current	I_{LP}	CTR21 Mode	13	—	60	mA
DC Ring Current[1]		DC current flowing through ring detection circuitry	—	—	7	µA
Ring Detect Voltage[2]	V_{RD}	RT = 0	11	—	22	V_{RMS}
Ring Detect Voltage[2]	V_{RD}	RT = 1	17	—	33	V_{RMS}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number[3]	REN		—	—	0.2	

Notes:
1. R25 and R26 installed.
2. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
3. C15, R14, Z2, and Z3 not installed. RZ = 0. See "Ringer Impedance" on page 25.

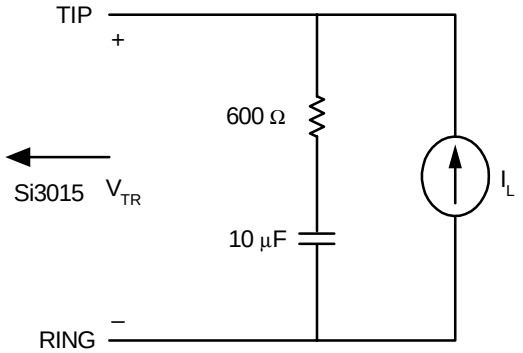


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 5 V

(V_D = 4.75 to 5.25 V, T_A = 0 to 70°C for K-Grade and –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		3.5	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	3.5	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog	I_A	V_A pin	—	0.3	1	mA
Power Supply Current, Digital[1]	I_D	V_D pin	—	14	18	mA
Total Supply Current, Sleep Mode[1]	$I_A + I_D$	PDN = 1, PDL = 0	—	1.3	2.5	mA
Total Supply Current, Deep Sleep[1,2]	$I_A + I_D$	PDN = 1, PDL = 1	—	0.04	0.5	mA

Notes:
1. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA). Clock frequency is f_{MAX}.
2. $\overline{\text{RGDT}}$ is not functional in this state.

Table 4. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70°C for K-Grade and –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog[1,2]	I_A	V_A pin	—	0.3	1	mA
Power Supply Current, Digital[3]	I_D	V_D pin	—	9	12	mA
Total Supply Current, Sleep Mode[3]	$I_A + I_D$	PDN = 1, PDL = 0	—	1.2	2.5	mA
Total Supply Current, Deep Sleep[3,4]	$I_A + I_D$	PDN = 1, PDL = 1	—	0.04	0.5	mA
Power Supply Voltage, Analog[1,5]	V_A	Charge Pump On	4.3	4.6	5.00	V

Notes:
1. Only a decoupling capacitor should be connected to V_A when the charge pump is on.
2. There is no I_A current consumption when the internal charge pump is enabled and only a decoupling capacitor is connected to the V_A pin.
3. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
4. $\overline{\text{RGDT}}$ is not functional in this state.
5. The charge pump must be used when V_D < 4.5 V. (Using the charge pump for all values of V_D is recommended.) When the charge pump is not used, V_A should be applied to the device before V_D is applied on power up if driven from separate supplies.

Table 5. AC Characteristics

(V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade and –40 to 85°C for B-Grade, see Figure 16 on page 15)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate[1]	Fs	Fs = F_{PLL2}/5120	7.2	—	11.025	KHz
PLL1 Output Clock Frequency[1]	F_{PLL1}	F_{PLL1} = F_{MCLK}*M1/N1	36	—	58	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[2]	V_{FS}	FULL = 0 (–1 dBm)	—	1	—	V_{peak}
		FULL = 1 (+3.2 dBm)[3]	—	1.58	—	V_{peak}
Receive Full Scale Level[2,4]	V_{FS}	FULL = 0 (–1 dBm)	—	1	—	V_{peak}
		FULL = 1 (+3.2 dBm)[3]	—	1.58	—	V_{peak}
Dynamic Range[5,6,7]	DR	ACT=0, DCT=10 (FCC) I_L=100 mA	—	82	—	dB
Dynamic Range[5,6,8]	DR	ACT=0, DCT=01 (Japan) I_L=20 mA	—	83	—	dB
Dynamic Range[5,6,7]	DR	ACT=1, DCT=11(CTR21) I_L=60 mA	—	84	—	dB
Transmit Total Harmonic Distortion[7,9]	THD	ACT=0, DCT=10 (FCC) I_L=100 mA	—	–85	—	dB
Transmit Total Harmonic Distortion[8,9]	THD	ACT=0, DCT=01 (Japan) I_L=20 mA	—	–76	—	dB
Receive Total Harmonic Distortion[8,9]	THD	ACT=0, DCT=01 (Japan) I_L=20 mA	—	–74	—	dB
Receive Total Harmonic Distortion[7,9]	THD	ACT=1, DCT=11 (CTR21) I_L=60 mA	—	–82	—	dB
Dynamic Range (call progress AOUT)	DR_{AO}	VIN = 1 kHz	60	—	—	dB
THD (call progress AOUT)	THD_{AO}	VIN = 1 kHz	—	1.0	—	%
AOUT Full Scale Level			—	0.75 V_A	—	V_{PP}
AOUT Output Impedance			—	10	—	kΩ
Mute Level (call progress AOUT)			–90	—	—	dBFS
Dynamic Range (Caller ID mode)	DR_{CID}	VIN = 1 kHz, –13 dBm	—	60	—	dB
Caller ID Full Scale Level (0 dB gain)	V_{CID}	MODE = 0	—	0.8	—	V_{PP}
Caller ID Full Scale Level (ARX = 00)	V_{CID}	MODE = 1	—	1.4	—	V_{PP}
Gain Accuracy[6,7]		2-W to SDO, ATX and ARX = 000, 001, or 010	–0.5	0	0.5	dB
Gain Accuracy[6,7]		2-W to SDO, ATX and ARX = 011, 1xx	–1	0	1	dB

Notes:

1. See Figure 28 on page 32.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. R2 should be changed to a 243 Ω resistor when the FULLSCALE bit (FULL) is set to 1 (Register 18, bit 7).
4. Receive full scale level will produce –0.9 dBFS at SDO.
5. DR = 20*log |Vin| + 20*log (RMS signal/RMS noise).
6. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
7. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
8. Vin = 1 kHz, –6 dBFS, Fs = 10300 Hz.
9. THD = 20*log (RMS distortion/RMS signal).

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 6.0	V
Input Current, Si3021 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Switching Characteristics — General Inputs

(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade and –40 to 85°C for B-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_{mc}	16.67	—	1000	ns
MCLK Duty Cycle	t_{dty}	40	50	60	%
Rise Time, MCLK	t_r	—	—	5	ns
Fall Time, MCLK	t_f	—	—	5	ns
MCLK Before $\overline{\text{RESET}}$ ↑	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}	250	—	—	ns
M0, M1 Before $\overline{\text{RESET}}$↑[3]	t_{mxr}	20	—	—	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D – 0.4$ V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 MCLK cycle times.
3. M0 and M1 are typically connected to V_D or GND and should not be changed during normal operation.

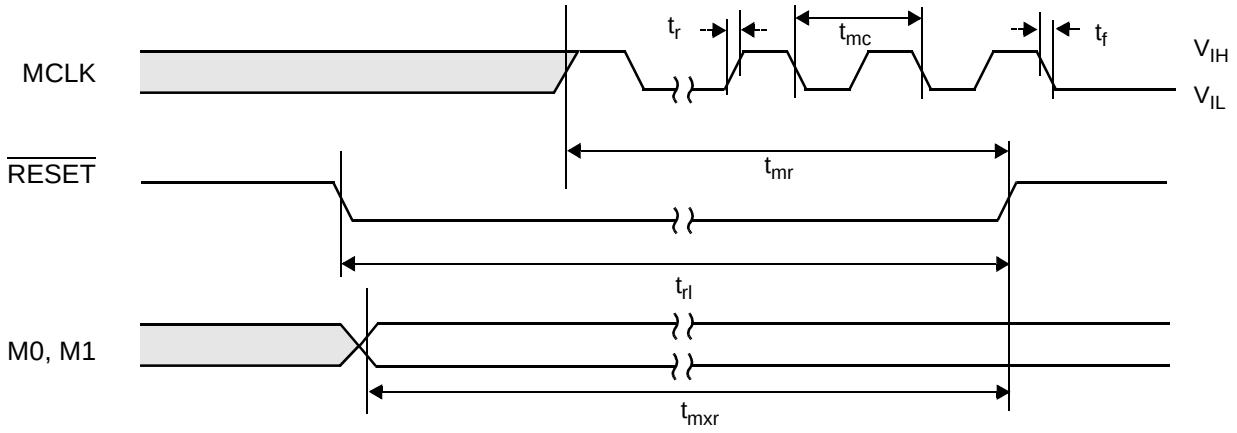


Figure 2. General Inputs Timing Diagram

Table 8. Switching Characteristics — Serial Interface (DCE = 0)
(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade and –40 to 85°C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK duty cycle	t_{dty}	—	50	—	%
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d1}	—	—	10	ns
Delay time, SCLK ↑ to SDO valid	t_{d2}	—	—	20	ns
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d3}	—	—	10	ns
Setup time, SDI before SCLK ↓	t_{su}	25	—	—	ns
Hold time, SDI after SCLK ↓	t_h	20	—	—	ns
Setup time, FC ↑ before SCLK ↑	t_{sfc}	40	—	—	ns
Hold time, FC ↑ after SCLK ↑	t_{hfc}	40	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D – 0.4$ V, V_{IL} = 0.4 V.					

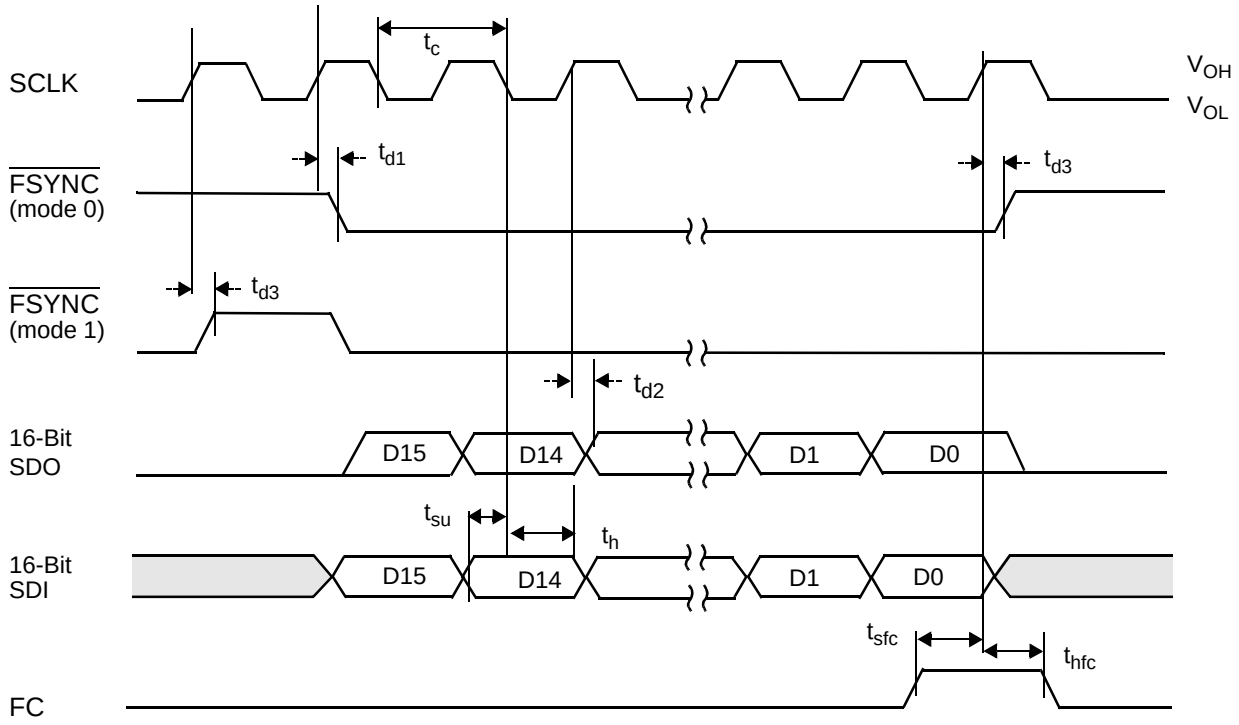


Figure 3. Serial Interface Timing Diagram (DCE = 0)

Table 9. Switching Characteristics — Serial Interface (DCE = 1, FSD = 0)
(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade and –40 to 85°C for B-Grade, C_L = 20 pF)

Parameter[1,2]	Symbol	Min	Typ	Max	Unit
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}	—	—	10	ns
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}	—	—	10	ns
Delay Time, SCLK ↑ to SDO valid	t_{d3}	—	—	20	ns
Delay Time, SCLK ↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Setup Time, SDO Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK ↓	t_h	20	—	—	ns
Setup Time, SDI Before SCLK ↓	t_{su2}	25	—	—	ns
Hold Time, SDI After SCLK ↓	t_{h2}	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D – 0.4$ V, V_{IL} = 0.4 V.
2. Refer to "Multiple Device Support" on page 34 for functional details.

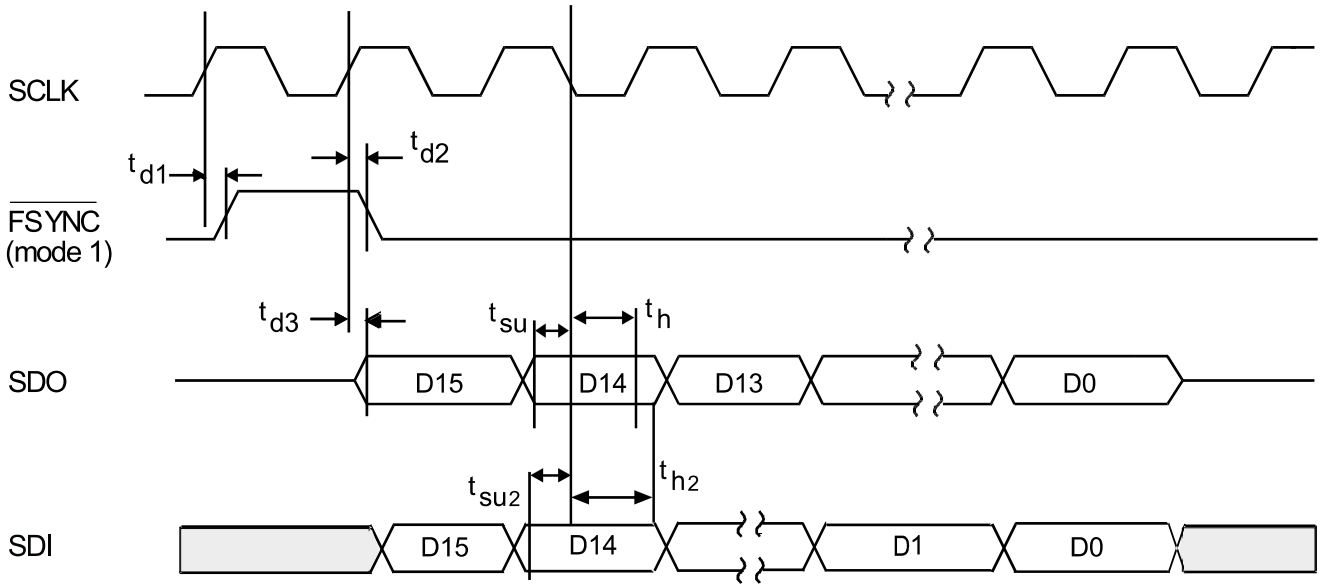


Figure 4. Serial Interface Timing Diagram (DCE = 1, FSD = 0)

Table 10. Switching Characteristics — Serial Interface (DCE = 1, FSD = 1)
(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade and –40 to 85°C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}	—	—	10	ns
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}	—	—	10	ns
Delay Time, SCLK ↑ to SDO valid	t_{d3}	$0.25t_c - 20$	—	$0.25t_c + 20$	ns
Delay Time, SCLK ↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{\text{RGDT}}$ ↓	t_{d5}	—	—	20	ns
Setup Time, SDO Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK ↓	t_h	20	—	—	ns
Setup Time, SDI Before SCLK	t_{su2}	25	—	—	ns
Hold Time, SDI After SCLK	t_{h2}	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V.
2. Refer to "Multiple Device Support" on page 34 for functional details.

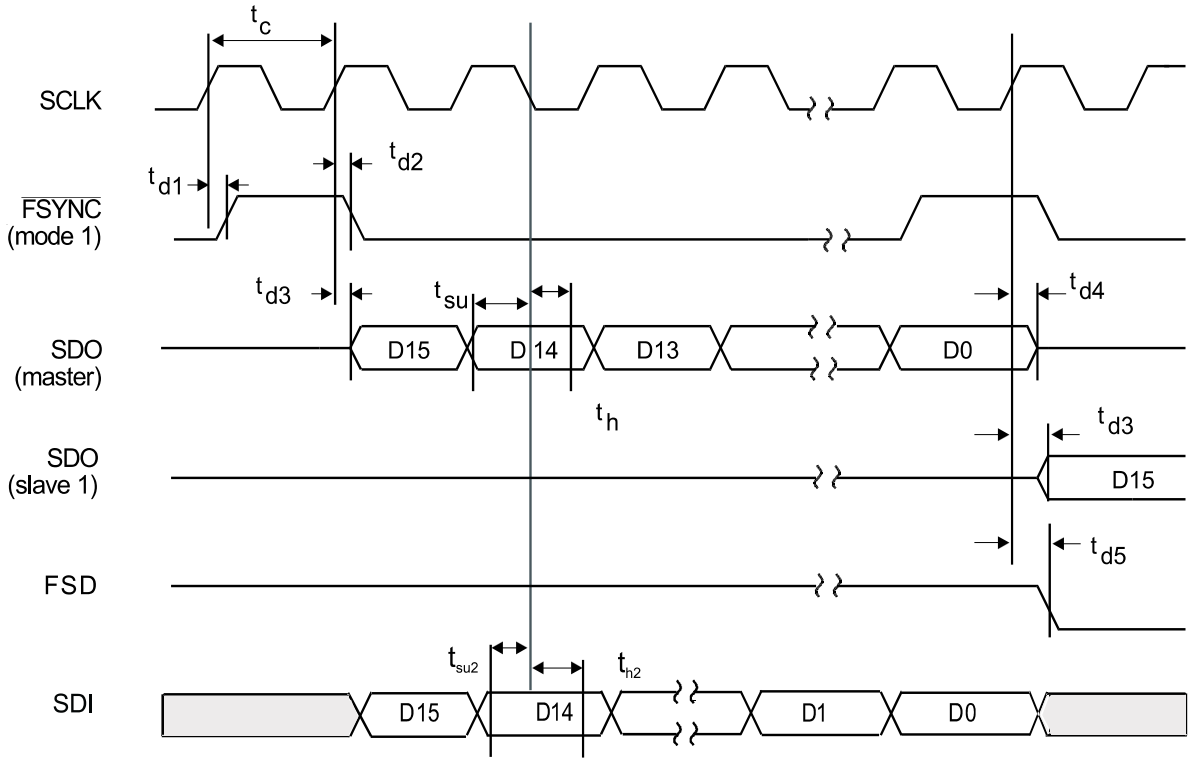


Figure 5. Serial Interface Timing Diagram (DCE = 1, FSD = 1)

Table 11. Digital FIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 5.25 V, Sample Rate = 8 kHz, T_A = 70°C for K-Grade and –40 to 85°C for B-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	sec
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 6, 7, 8, and 9.					

Table 12. Digital IIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 5.25 V, Sample Rate = 8 kHz, T_A = 70°C for K-Grade and –40 to 85°C for B-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	sec
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 10, 11, 12, and 13. Figures 14 and 15 show group delay versus input frequency.					

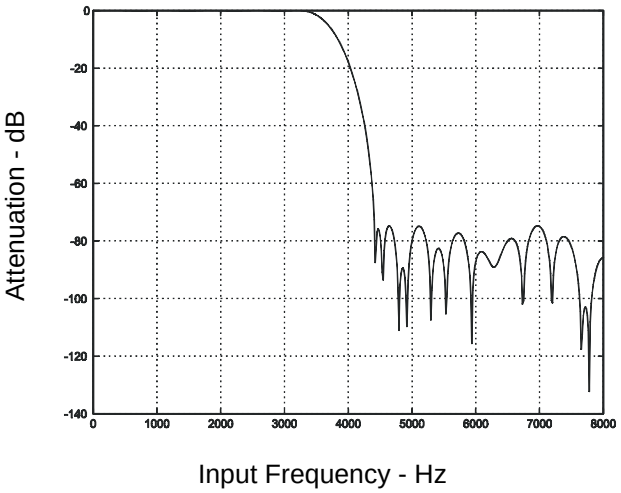


Figure 6. FIR Receive Filter Response

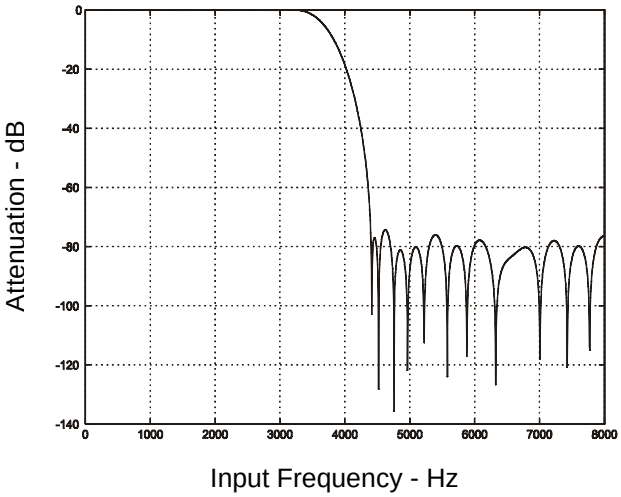


Figure 8. FIR Transmit Filter Response

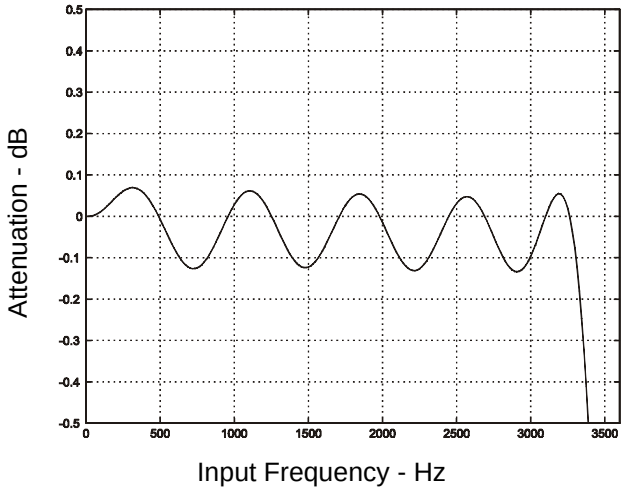


Figure 7. FIR Receive Filter Passband Ripple

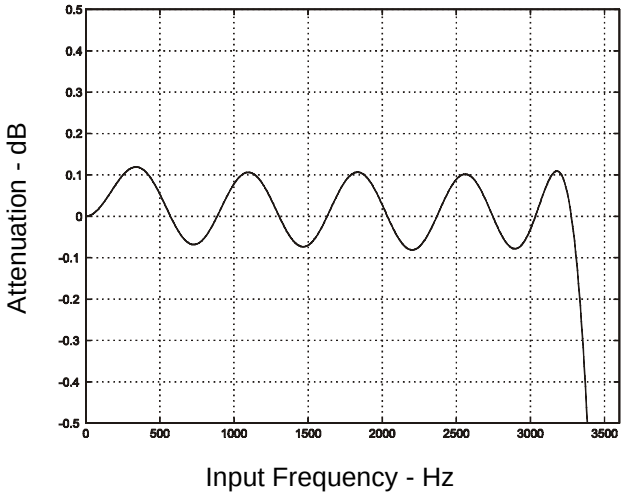


Figure 9. FIR Transmit Filter Passband Ripple

For Figures 6–9, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)} = 0.4125\ Fs$

$F_{(-3\ dB)} = 0.45\ Fs$

where Fs is the sample frequency.

For Figures 10–13, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(-3\ dB)} = 0.45\ Fs$

where Fs is the sample frequency.

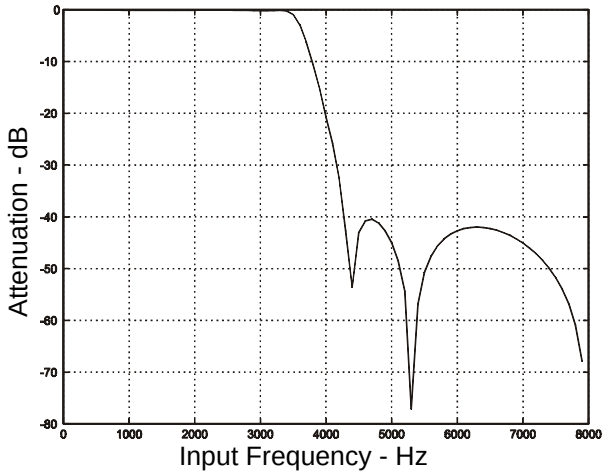


Figure 10. IIR Receive Filter Response

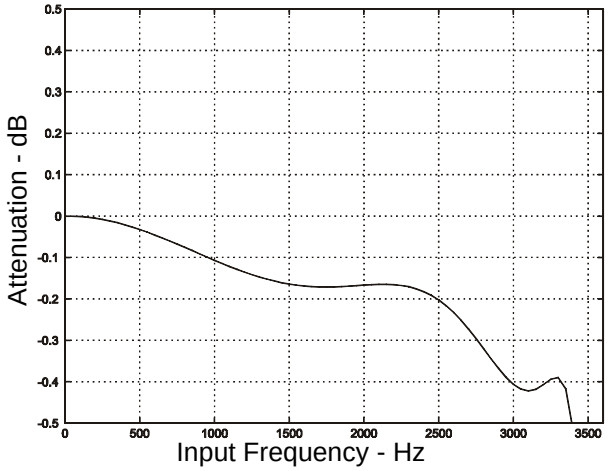


Figure 13. IIR Transmit Filter Passband Ripple

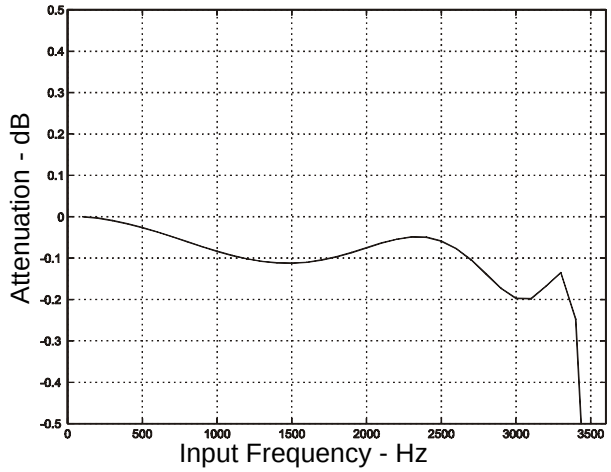


Figure 11. IIR Receive Filter Passband Ripple

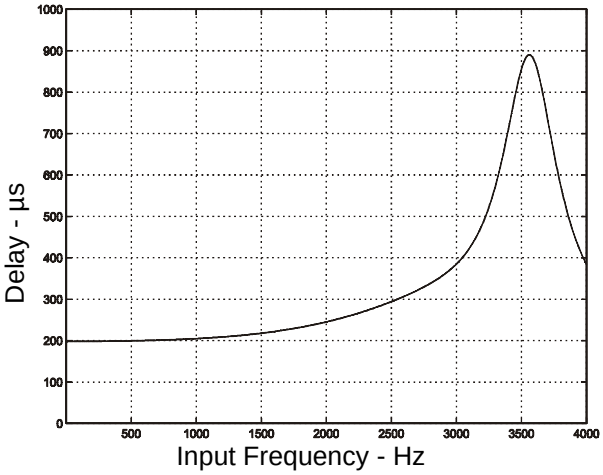


Figure 14. IIR Receive Group Delay

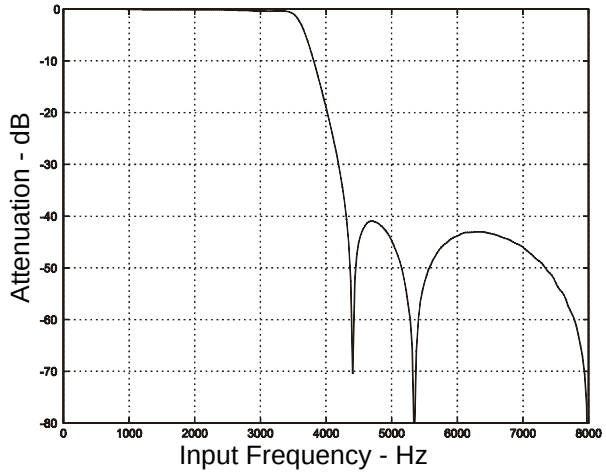


Figure 12. IIR Transmit Filter Response

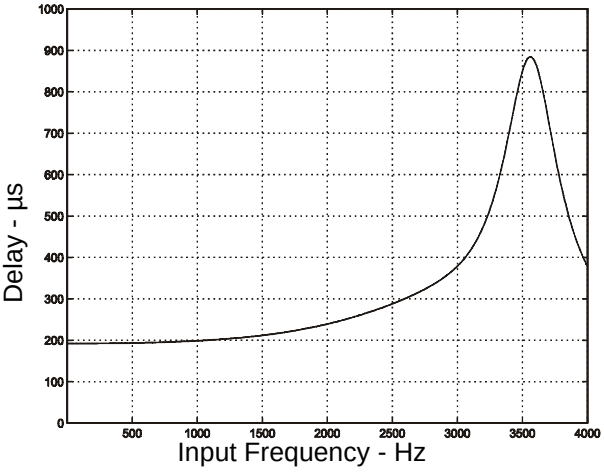
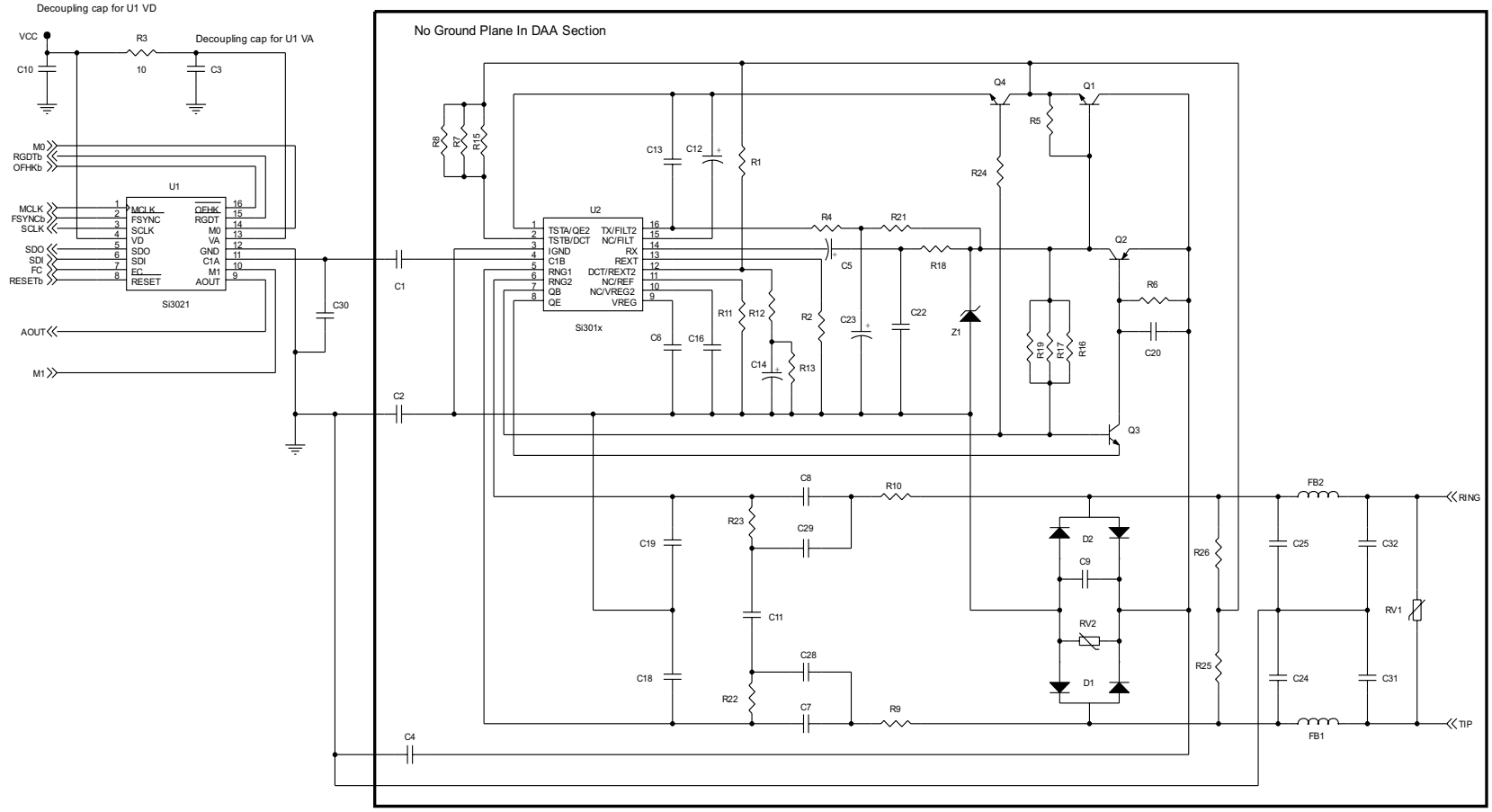


Figure 15. IIR Transmit Group Delay



Note 1: This design targets two basic builds:
- An FCC and JATE compliant design using the Si3035 chipset.
- A worldwide design using the Si3044 chipset.

Note 2: R12, R13 and C14 are only required if complex AC termination is used (ACT bit = 1).

Note 3: See "Ringer Impedance" section for optional Czech Republic support.

Note 4: See "Billing Tone Detection" section for optional billing tone filter (Germany, Switzerland, South Africa).

Note 5: See Appendix for applications requiring UL 1950 3rd edition compliance.

Figure 16. Typical Applications Circuit for the Dual Design Si3044 and Si3035

Bill of Materials

Table 13. Global Component Values—Si3044 Chipset

Component	Value	Suppliers
C1,C4	150 pF, 3 kV, X7R,±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C2,C11,C23,C28,C29	Not Installed	
C3,C13[1]	0.22 µF, 16 V, X7R, ±20%	
C5	0.1 µF, 50 V, Elec/Tant, ±20%	
C6,C10,C16	0.1 µF, 16 V, X7R, ±20%	
C7,C8	1800 pF, 250 V, X7R, ±20%	Novacap, Johanson, Murata, Panasonic
C9	22 nF, 250 V, X7R, ±20%	
C12	1.0 µF, 16 V, Tant, ±20%	
C14	0.68 µF, 16 V, X7R/Elec/Tant, ±20%	
C18,C19	12 nF, 16 V, X7R, ±20%	
C20	0.01 µF, 16 V, X7R, ±20%	
C22	1800 pF, 50 V, X7R, ±20%	
C24,C25,C31,C32[2]	1000 pF, 3 kV, X7R, ±10%	
C30[3]	Not Installed	
D1,D2[4]	Dual Diode, 300 V, 225 mA	Central Semiconductor
FB1,FB2	Ferrite Bead	Murata
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild
Q4[5]	BCP56T1, NPN, 80 V, 1/2 W	OnSemiconductor, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2[6]	Not Installed	
R1,R4,R21,R22,R23	Not Installed	
R2[7]	402 Ω, 1/16 W, ±1%	
R3[8]	Not Installed	
R5	100 kΩ, 1/16 W, ±1%	
R6	120 kΩ, 1/16 W, ±5%	
R7,R8,R15,R16,R17,R19[9]	4.87 kΩ, 1/4 W, ±1%	
R9,R10	15 kΩ, 1/10 W, ±5%	
R11	10 kΩ, 1/16 W, ±1%	
R12	78.7 Ω, 1/16 W, ±1%	
R13	215 Ω, 1/16 W, ±1%	
R18	2.2 kΩ, 1/10 W, ±5%	
R24	150 Ω, 1/16 W, ±5%	
R25,R26	10 MΩ, 1/16 W, ±5%	
U1	Si3021	Silicon Labs
U2	Si3015	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	Vishay, Motorola, Rohm

Notes:

1. C13 is used to ensure compliance with on-hook pulse dialing and spark quenching requirements in countries such as Australia and South Africa. If this is not a concern, a 0.1 µF cap may be used.
2. Alternate population option is C24, C25 (2200 pF, 3 kV, X7R, ±10% and C31, C32 not installed).
3. Install only if needed for improved radiated emissions performance (10 pF, 16 V, NPO, ±10%).
4. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.).
5. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
6. RV2 can be installed to improve performance from 2500 V to 3500 V for multiple longitudinal surges (240 V, MOV).
7. If supporting +3.2 dBFS voice applications, R2 should be 243 Ω and set the FULLSCALE bit (Reg 18[7]).
8. If the charge pump is not enabled (with the CPE bit in Register 6), V_A must be 4.75 to 5.25 V. R3 can be installed with a 10 Ω, 1/10 W, ±5% if V_D is also 4.75 to 5.25 V.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.62 kΩ, 3/4 W, ±1%.

Table 14. FCC Component Values—Si3035 Chipset

Component[1]	Value	Suppliers
C1,C4	150 pF, 3 kV, X7R,±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C2	Not Installed	
C3	0.22 µF, 16 V, X7R, ±20%	
C5	1.0 µF, 16 V, Elec/Tant, ±20%	
C6,C10,C16	0.1 µF, 16 V, X7R, ±20%	
C9,C28,C29	15 nF, 250 V, X7R, ±20%	Novacap, Johanson, Murata, Panasonic
C11	39 nF, 16 V, X7R, ±20%	
C7,C8,C12,C13,C14 C18,C19,C20,C22,C23[2]	Not Installed	
C24,C25,C31,C32[3]	1000 pF, 3 kV, X7R, ±10%	Novacap, Venkel, Johanson, Murata, Panasonic
C30[4]	Not Installed	
D1,D2[5]	Dual Diode, 300 V, 225 mA	Central Semiconductor
FB1,FB2	Ferrite Bead	Murata
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild
Q4	Not Installed	
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2	240 V, MOV	Panasonic
R1	51 Ω, 1/2 W, ±5%	
R2	15 Ω, 1/4 W, ±5%	
R3[6]	Not Installed	
R4,R18,R21	301 Ω, 1/10 W, ±1%	
R5,R6	36 kΩ, 1/10 W, ±5%	
R7,R8,R11[2],R12,R13,R15 R16,R17,R19,R24,R25,R26	Not Installed	
R9,R10	2 kΩ, 1/10 W, ±5%	
R22,R23	20 kΩ, 1/10 W, ±5%	
U1	Si3021	Silicon Labs
U2	Si3012	Silicon Labs
Z1	Zener Diode, 18 V	Vishay, Motorola, Rohm

Notes:

1. The following reference designators were intentionally omitted: C15, C17, C21, C26, C27, R14, and R20.
2. If JATE support is required using the Si3035 chipset, C23 should be populated with a 0.1 µF, 16 V, Tant/Elec/X7R, ±20% and R11 should be populated with a 2.7 nF, 16 V, X7R, ±20% capacitor.
3. Alternate population option is C24, C25 (2200 pF, 3 kV, X7R, ±10% and C31, C32 not installed).
4. Install only if needed for improved radiated emissions performance (10 pF, 16 V, NPO, ±10%).
5. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.).
6. If the charge pump is not enabled (with the CPE bit in Register 6), V_A must be 4.75 to 5.25 V. R3 can be installed with a 10 Ω, 1/10 W, ±5% if V_D is also 4.75 to 5.25 V.

Analog Output

Figure 17 illustrates an optional application circuit to support the analog output capability of the Si3044 for call progress monitoring purposes. The ARM bits in Register 6 allow the receive path to be attenuated by 0 dB, –6 dB, or –12 dB. The ATM bits, which are also in Register 6, allow the transmit path to be attenuated by –20 dB, –26 dB, or –32 dB. Both the transmit and receive paths can also be independently muted.

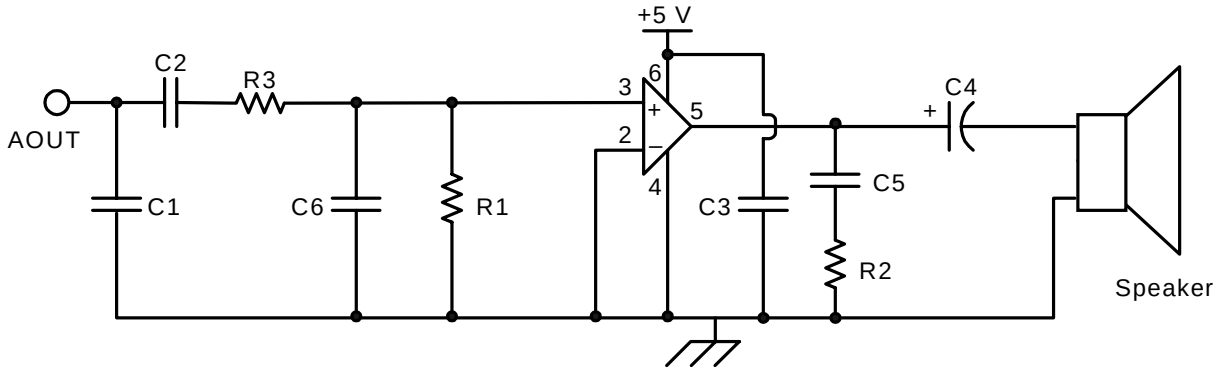


Figure 17. Optional Connection to AOUT for a Call Progress Speaker

Table 15. Component Values—Optional Connection to AOUT

Symbol	Value
C1	2200 pF, 16 V, ±20%
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	10 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/10 W, ±5%
U1	LM386

Functional Description

The Si3044 is an integrated Direct Access Arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The device implements Silicon Laboratories' proprietary ISOcap technology which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two 16-pin small outline integrated circuit (SOIC) packages.

The Si3044 chipset can be fully programmed to meet international requirements and is compliant with FCC, CTR21, JATE, and various other country-specific PTT specifications as shown in Table 17. In addition, the Si3044 has been designed to meet the most stringent worldwide requirements for out-of-band energy, emissions, immunity, lightning surges, and safety. Typical Si3044 designs implement a dual layout (see Figure 16) capable of two population options:

- FCC Compliant Population—This population option removes the external devices needed to support non-FCC countries. The FCC/JATE DAA Si3035 chipset is used.
- Globally Compliant Population—This population option targets global DAA requirements. The Si3044 international DAA chipset is populated, and the external devices required for the FCC-only population option are removed. *This population option supports FCC-compliant countries as well as non-FCC-compliant countries.*

New Features

The Si3044 enhanced global DAA offers a number of new features not provided in the Si3034 global DAA. These include line voltage monitoring, improved detection of an off-hook parallel phone, lower current in on-hook line monitor mode, and higher full-scale transmit/receive levels for voice applications. Table 16 summarizes the Si3044 features.

Upgrading from Si3034 to Si3044

The Si3044 is pin compatible with the Si3034; therefore, it can be used in existing designs that use the Si3034 without requiring any board layout changes. A few value changes to external components are required to utilize the new line-side device. Additionally, if line voltage monitoring is needed, two 10M Ω resistors (R25 and R26) must be added as specified in the recommended application circuit.

When transitioning from the Si3034 to the Si3044, the application must be modified as follows:

- Change the value of C12 from 0.22 µF to 1 µF.
- Change the value of C13 from 0.47 µF to 0.22 µF.
- Add R25 and R26 as specified in the application circuit (required for line voltage monitor only).
- Change the value of R5 from 36 kΩ to 100 kΩ (required for line voltage monitor only).
- Check for use of CTRO (CTR21 overload) bit (Register 19) in the Si3034 design. This bit is now part of the LVCS (line voltage current sense) bits in the Si3044.
- Check for use of LCS (loop current sense) bits in the Si3034 design. These bits are decoded differently in the Si3044. (See the LCS bits in Register 12.)
- Check for use of the LIM[0] bit (Register 17) in the Si3034. This bit is redefined as the OPE (overload protect enable) in the Si3044. The Si3044 will not operate as assigned if this bit is set during off-hook.
- Check for use of the BTD, ROV, and OVL bits (registers 17, 19). These bits are always enabled on the Si3044. (The Si3034 requires BTE to be enabled.)
- Check for use of the VOL bits (Register 18). These bits are redefined in the Si3044.
- If the FULLSCALE bit is used to enable +3.2 dBm fullscale operation, R2 should be changed from 402 Ω to 243 Ω.

Table 16. New Si3044 Features

Description	Si3034	Si3044
Line Voltage Monitor (On-Hook)	—	2.75 V/bit
Improved Parallel Handset Detection	—	Yes
Loop Current Monitor (Off-Hook)	6 mA/bit	3 mA/bit
TX/RX Full Scale	–1 dBm	–1 dBm/3.2 dBm*
On-Hook Line Monitor Current	450 µA	7 µA

***Note:** Full scale level is selectable via the FULL bit (Register 18, bit 7). R2 must also be changed to a 243 Ω resistor to support the +3.2 dBm full scale level.

Table 17. Country Specific Register Settings

Register	16					17	18
Country	**OHS**	**ACT**	**DCT[1:0]**	**RZ**	**RT**	**LIM**	**VOL**
Australia[1]	1	1	01	0	0	0	0
Bulgaria	0	0 or 1	10	0	0	0	0
China[1]	0	0	01	0	0	0	0
CTR21[1,2]	0	0 or 1	11	0	0	1	0
Czech Republic[3]	0	1	10	0	0	0	0
FCC	0	0	10	0	0	0	0
Hungary	0	0	10	0	0	0	0
Japan[1]	0	0	01	0	0	0	0
Malaysia[1,4]	0	0	01	0	0	0	0
New Zealand	0	1	10	0	0	0	0
Philippines[1]	0	0	01	0	0	0	1
Poland[5]	0	0	10	1	1	0	0
Singapore	0	0	10	0	0	0	0
Slovakia	0	0 or 1	10	0	0	0	0
Slovenia	0	1	10	0	0	0	0
South Africa[5]	1	1	10	1	0	0	0
South Korea[1,5]	0	0	01	1	0	0	0

Note:
1. See "DC Termination Considerations" on page 24 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. See "Ringer Impedance" on page 25.
4. Supported for loop current ≥ 20 mA.
5. The RZ bit in Register 16 should only be set for Poland, South Africa and South Korea if the ringer impedance network (C15, R14, Z2, Z3) is not populated.

Initialization

When the Si3044 is initially powered up, the $\overline{\text{RESET}}$ pin should be asserted. When the $\overline{\text{RESET}}$ pin is deasserted, the registers will have default values. This reset condition guarantees the line-side chip (Si3015) is powered down with no possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined below:

1. Program the PLLs with registers 7 to 9 (N1[7:0], M1[7:0], N2[3:0], and M2[3:0]) to the appropriate divider ratios for the supplied MCLK frequency and desired sample rate, as defined in "Clock Generation Subsystem" on page 31.
2. Wait until the PLLs are locked. This time is between 100 µS and 1 ms.
3. Write an 80H into Register 6. This enables the charge pump for the V_A pin, powers up the line-side chip (Si3015), and enables the AOUT for call progress monitoring.
4. Set the desired line interface parameters (i.e., DCT[1:0], ACT, OHS, RT, LIM[1:0], and VOL) as defined by "Country Specific Register Settings" shown in Table 17.

After this procedure is complete, the Si3044 is ready for ring detection and off-hook.

On-Chip Charge Pump

The Si3044 has an on-chip charge pump that can produce the V_A supply needed by the ISOcap communication link. This on-chip power supply can be enabled by setting bit 7 in Register 6 to 1. If the on-chip charge pump is used, R3 should not be populated.

Before enabling the line-side chip, care should be taken to ensure it is properly powered. The V_A supply may be powered from the digital power supply (V_D) if it is at least 4.75 V, and R3 is populated. A separate 5 V power supply may also be used for V_A independent of the digital supply, in which case R3 should not be populated. If neither of these two options are viable, the

on-chip charge pump should be enabled, and R3 should not be populated.

Isolation Barrier

The Si3044 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' proprietary ISOcap signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 16 on page 15, the C1, C4, C24, and C25 capacitors isolate the Si3021 (DSP-side) from the Si3015 (line-side). All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier.

The ISOcap communications link is disabled by default. To enable it, the PDL bit in Register 6 must be cleared. No communication between the Si3021 and Si3015 can occur until this bit is cleared. The clock generator **must** be programmed to an acceptable sample rate prior to clearing the PDL bit.

Transmit/Receive Full Scale Level

The Si3044 supports programmable maximum transmit and receive levels. The full scale TX/RX level is established by writing the FULL bit in Register 18. With FULL = 1, the full scale TX/RX level is increased to 3.2 dBm to support certain FCC voice applications which require higher TX/RX levels. When FULL = 1, R2 must be changed from 402 Ω to 243 Ω. The default full scale value is –1 dBm (FULL = 0) which is backward compatible with the Si3034. Note that this higher TX/RX full scale mode must be used in FCC/600 Ω termination mode.

Parallel Handset Detection

The Si3044 is capable of detecting a parallel handset going off-hook. When the Si3044 is off-hook, the loop current can be monitored via the LVCS bits. A significant drop in loop current can signal a parallel handset going off-hook. If a parallel handset causes the LVCS bits to read all zeroes, the Drop-Out Detect (DOD) bit may be checked to verify a valid line still exists.

When on-hook, the LVCS bits may also be read to determine the line voltage. Significant drops in line voltage may also be used to detect a parallel handset. For the Si3044 to operate in parallel with another handset, the parallel handset must have a sufficiently high DC termination to support two off-hook DAAs on the same line. The OFF bit in Register 16 is designed to improve parallel handset operation by changing the DC impedance from 50 Ω to 800 Ω and reducing the DCT pin voltage.

Line Voltage/Loop Current Sensing

The Si3044 has the ability to measure both line voltage and loop current. The five bit LVCS register reports line voltage measurements when on-hook, loop current measurements when off-hook, or on-hook line monitor data depending on the state of the MODE, OH, and ONHM bits.

Using the LVCS bits, the user can determine the following:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- Detect if there is an overload condition which could damage the DAA (see overload protection feature).

Line Voltage Measurement

The Si3044 reports the line voltage with the LVCS bits in Register 19. LVCS has a full scale of 87 V with an LSB of 2.75 V. The first code (0 → 1) is skewed such that a 0 indicates that the line voltage is < 3 V. The accuracy of the LVCS bits is ±20%. The user can read these bits directly through the LVCS register when on-hook and the MODE bit (Register 18, bit 2) is set to 1. A typical transfer function is shown in Figure 18.

Loop Current Measurement

When the Si3044 is off-hook, the LVCS bits measure loop current in 3 mA/bit resolution. These bits enable the user to detect another phone going off-hook by monitoring the DC loop current. The line voltage current sense transfer function is shown in Figure 19 and is detailed in Table 18.

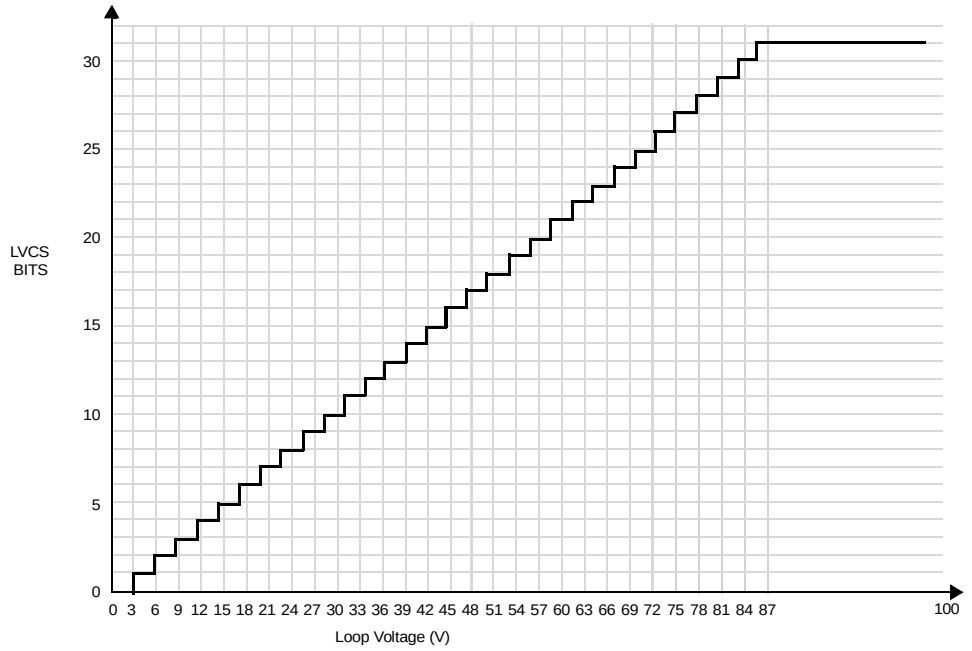


Figure 18. Typical Loop Voltage LVCS Transfer Function

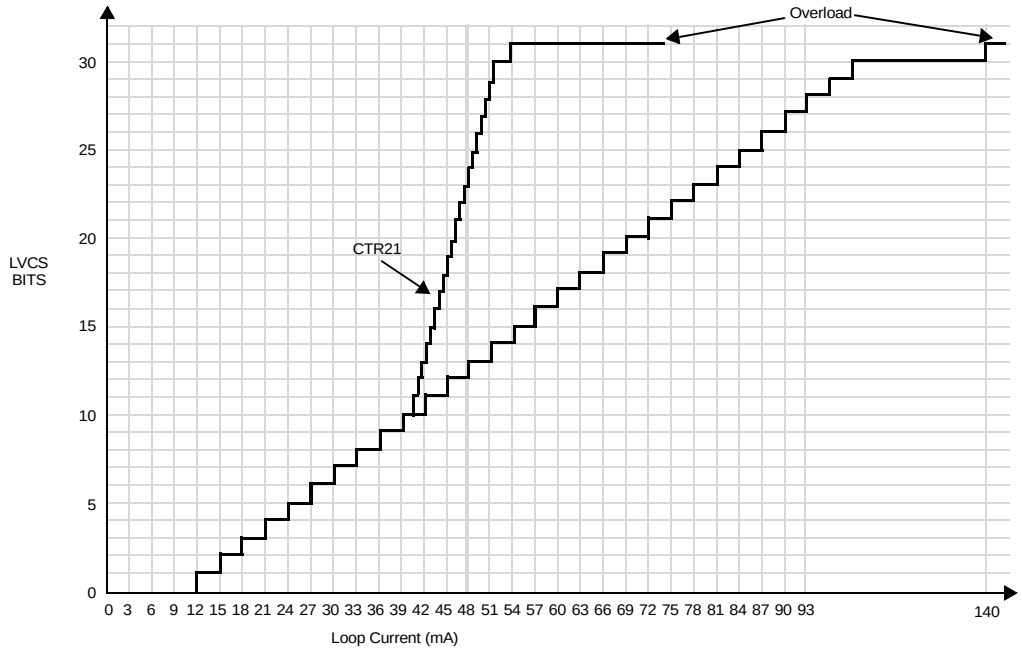


Figure 19. Typical Loop Current LVCS Transfer Function

Table 18. Loop Current Transfer Function

LVCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DOD bit (Register 19, bit 1) to determine if a line is still connected.
00001	Minimum line current for normal operation.
11111	Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21. Overload > 54 mA in CTR21 mode.

Off-Hook

The communication system generates an off-hook command by applying a logic 0 to the OFHK pin or by setting the OH bit in Register 5.The OFHK pin must be enabled by setting the OHE bit in Register 5. With OFHK at logic 0, the system is in an off-hook state. Before setting the OH bit, the on-hook line monitor feature should be disabled. (See "On-Hook Line Monitor" on page 28.) When using the OFHK pin, the on-hook line monitor feature should be disabled and at least one sample period should pass before driving the OFHK pin low.

The off-hook state is used to seize the line for incoming/ outgoing calls and can also be used for pulse dialing. With OFHK at logic 1, negligible DC current flows through the hookswitch. When a logic 0 is applied to the OFHK pin, the hookswitch transistor pair, Q1 & Q2, turn on. This applies a termination impedance across TIP and RING and causes DC loop current to flow. The termination impedance has both an AC and DC component.

When executing an off-hook sequence, the Si3044 requires 1548/Fs seconds to complete the off-hook and provide phone-line data on the serial link. This includes the 12/Fs filter group delay. If necessary, for the shortest delay, a higher Fs may be established prior to executing the off-hook, such as an Fs of 10.286 kHz. The delay allows for line transients to settle prior to normal use.

DC Termination

The Si3044 has four programmable DC termination modes which are selected with the DCT[1:0] bits in Register 16.

FCC mode (DCT[1:0] = 10 b), shown in Figure 20, is the default DC termination mode and supports a transmit full scale level of –1 dBm at TIP and RING. This mode meets FCC requirements in addition to the requirements of many other countries.

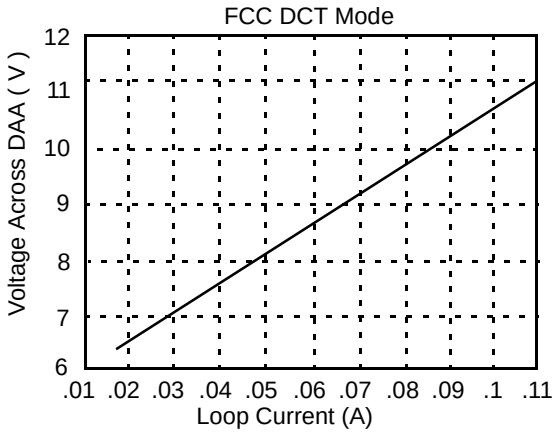


Figure 20. FCC Mode I/V Characteristics

CTR21 mode (DCT[1:0] = 11 b), shown in Figure 21, provides current limiting while maintaining a transmit full scale level of –1 dBm at TIP and RING. In this mode, the DC termination will current limit before reaching 60 mA.

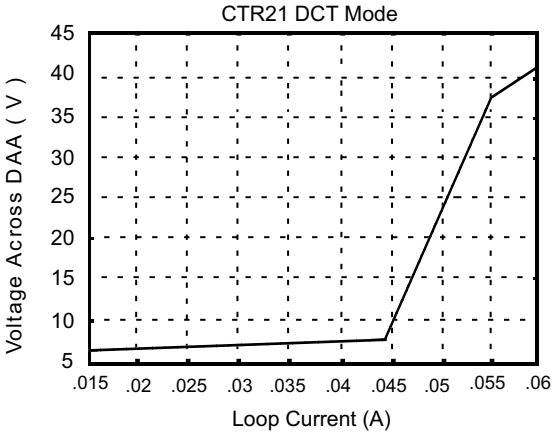


Figure 21. CTR21 Mode I/V Characteristics

Japan mode (DCT[1:0] = 01 b), shown in Figure 22, is a lower voltage mode and supports a transmit full scale level of –2.71 dBm. Higher transmit levels for DTMF dialing are also supported. See "DTMF Dialing" on page 26. The low voltage requirement is dictated by countries such as Japan and Malaysia.

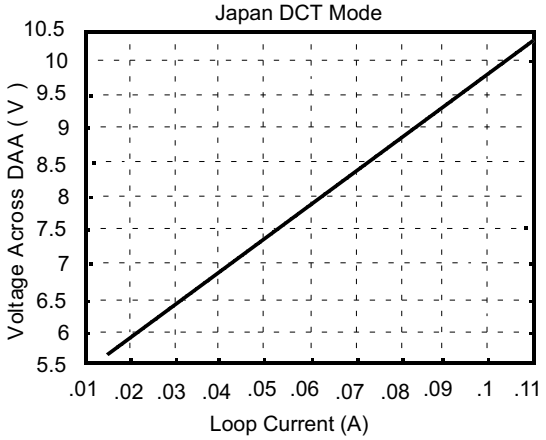


Figure 22. Japan Mode I/V Characteristics

Low Voltage mode (DCT[1:0] = 00b), shown in Figure 23, is the lowest line voltage mode supported on the Si3044, with a transmit full scale level of –5 dBm. Higher transmit levels for DTMF dialing are also supported. See “DTMF Dialing”. This low voltage mode is offered for situations that require very low line voltage operation. It is important to note that this mode should only be used when necessary, as the dynamic range will be significantly reduced and thus the Si3044 will not be able to transmit or receive large signals without clipping them.

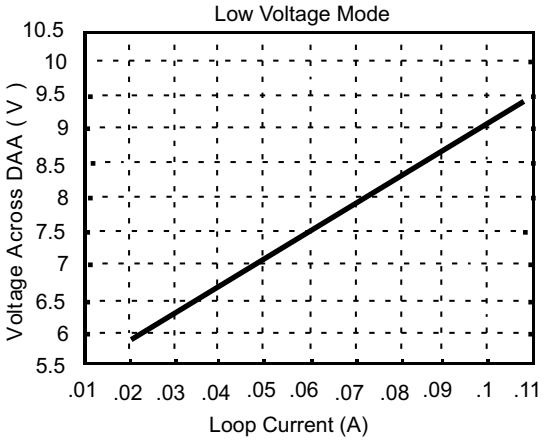


Figure 23. Low Voltage Mode I/V Characteristics

DC Termination Considerations

Under certain line conditions, it may be beneficial to use other DC termination modes not intended for a particular world region. For instance, in countries that comply with the CTR21 standard, improved distortion characteristics can be seen for very low loop current lines by switching to FCC mode. Thus, after going off-hook in CTR21 mode, the loop current monitor bits (LVCS[4:0]) may be used to measure the loop current, and if LVCS[4:0] < 6, it is recommended that FCC mode be used.

Additionally, for very low voltage countries, such as Japan and Malaysia, the following procedure should be used to optimize distortion characteristics and maximize transmit levels:

1. When first going off-hook, use the Low Voltage mode with the VOL bit (Register 18, bit 4) set to 1.
2. Measure the loop current using the LVCS[4:0] bits.
3. If LVCS[4:0] ≤ 2, maintain the current settings and proceed with normal operation.
4. If LVCS[4:0] > 2 or < 6, switch to Japan mode, leave the VOL bit set, and proceed with normal operation.
5. If LVCS[4:0] ≥ 6, switch to FCC mode, set the VOL bit to 0, and proceed with normal operation.

Finally, Australia has separate DC termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial off-hook. This will satisfy the Australian DC termination requirements.

AC Termination

The Si3044 has two AC Termination impedances which are selected with the ACT bit in Register 16.

ACT=0 is a real, nominal 600 Ω termination which satisfies the impedance requirements of FCC part 68, JATE, and other countries. This real impedance is set by circuitry internal to the Si3044 as well as the resistor R2 connected to the REXT pin.

ACT=1 is a complex impedance which satisfies the impedance requirements of Australia, New Zealand, South Africa, CTR21, and some European NET4 countries such as the UK and Germany. This complex impedance is set by circuitry internal to the Si3044 as well as the complex network formed by R12, R13, and C14 connected to the REXT2 pin.

Ring Detection

The ring signal is capacitively coupled from TIP and RING to the RNG1 and RNG2 pins. The Si3044 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal as well as the ring signal. See “Caller ID” on page 28. The ring detection threshold is programmable with the RT bit in Register 16.

The ring detector output can be monitored in one of three ways. The first method uses the $\overline{\text{RGDT}}$ pin. The second method uses the register bits RDTP, RDTN, and RDT in Register 5. The final method uses the SDO output.

The DSP must detect the frequency of the ring signal in order to distinguish a ring from pulse dialing by telephone equipment connected in parallel.

The ring detector mode is controlled by the RFWE bit in Register 18. When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ringing signals are detected. A positive ringing signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. RNG1 and RNG2 are pins 5 and 6 of the Si3015. Conversely, a negative ringing signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2.

When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

When the RFWE bit is 0, the $\overline{\text{RGDT}}$ pin will toggle active low when the ring signal is positive. When the RFWE bit is 1, the $\overline{\text{RGDT}}$ pin will toggle active low when the ring signal is positive or negative. This makes the ring signal appear to be twice the frequency of the ringing waveform.

The second method uses the ring detect bits (RDTP, RDTN, and RDT). The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. Whenever the signal on RNG1-RNG2 is above the positive ring threshold the RDTP bit is set. Whenever the signal on RNG1-RNG2 is below the negative ring threshold the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is a 0 or a 1, a positive ringing signal will set the RDT bit for a period of time. The RDT bit will not be set for a negative ringing signal.

The RDT bit acts as a one shot. Whenever a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter counting down to zero, then the RDT bit will return to zero. The length of this count (in seconds) is 65536 divided by the sample rate. The RDT will also be reset to zero by an off-hook event.

The third method uses the serial communication interface to transmit ring data. If the ISOcap is active (PDL=0) and the device is not off-hook or not in on-hook line monitor mode, the ring data will be presented on SDO. The waveform on SDO depends on the state of the RFWE bit.

When RFWE is 0, SDO will be –32768 (8000h) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, SDO will transition to +32767 while the ring signal is positive, then go back to –32768 while the ring is near zero and negative. Thus a near square wave is presented on SDO that swings from –32768 to +32767 in cadence with the ring signal.

When RFWE is 1, SDO will sit at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring goes positive, SDO will transition to +32767. When the ring signal goes near zero, SDO will remain near 1228. Then as the ring goes negative, the SDO will transition to –32768. This will repeat in cadence with the ring signal.

The best way to observe the ring signal on SDO is simply to observe the MSB of the data. The MSB will toggle in cadence with the ring signal independent of the ring detector mode. This is adequate information for determining the ring frequency. The MSB of SDO will toggle at the same frequency as the ring signal.

Ringer Impedance

The ring detector in a typical DAA is AC coupled to the line with a large, 1 uF, 250 V decoupling capacitor. The ring detector on the Si3044 is also capacitively coupled to the line, but it is designed to use smaller, less expensive 1.8 nF capacitors. Inherently, this network produces a very high ringer impedance to the line on the order of 800 to 900 kΩ. This value is acceptable for the majority of countries, including FCC and CTR21.

Several countries including the Czech Republic, Poland, South Africa and South Korea, require a maximum ringer impedance. For Poland, South Africa, and South Korea, the maximum ringer impedance specification can be met with an internally synthesized impedance by setting the RZ bit in Register 16.

For Czech Republic designs, an additional network comprised of C15, R14, Z2, and Z3 is required. (See Figure 24 and Table 19.) This network is not required for any other country. However, if this network is installed, the RZ bit should not be set for any country.

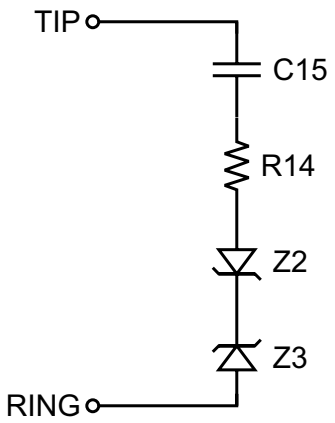


Figure 24. Ringer Impedance Network

Table 19. Component Values—Optional Ringer Impedance Network

Symbol	Value
C15	1 µF, 250 V
R14	7.5 kΩ, 1/4 W
Z2,Z3	5.6 V

DTMF Dialing

In CTR21 DC termination mode, the DIAL bit in Register 18 should be set during DTMF dialing if the LVCS[4:0] bits are less than 12. Setting this bit increases headroom for large signals. This bit should not be used during normal operation, or if the LVCS[4:0] bits are greater than 11.

In Japan DC termination mode, the Si3021 device attenuates the transmit output by 1.7dB to meet headroom requirements. Similarly, in Low Voltage termination mode, the Si3021 device attenuates the transmit output by 4 dB. However, when DTMF dialing is desired in these modes, this attenuation must be removed. This is achieved by entering the FCC DC termination mode and setting either the FJM or the FLVM bits. When in the FCC DC termination modes, these bits will enable the respective lower loop current termination modes without the associated transmit attenuation. Increased distortion may be observed, which is acceptable during DTMF dialing. After DTMF dialing is complete, the attenuation should be enabled by returning to either the Japan DC termination mode (DCT[1:0] = 01b) or the Low Voltage termination mode (DCT[1:0] = 00b). The FJM and the FLVM bits have no effect in any other termination mode other than the FCC DC termination mode.

Higher DTMF levels may also be achieved if the amplitude is increased and the peaks of the DTMF signal are clipped at digital full scale (as opposed to wrapping). Clipping the signal will produce some distortion and intermodulation of the signal. Generally, somewhat increased distortion (between 10–20%) is acceptable during DTMF signaling. Several dB higher DTMF levels can be achieved with this technique, compared with a digital full scale peak signal.

Pulse Dialing

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have very tight specifications for pulse fidelity, including make and break times, make resistance, and rise and fall times. In a traditional solid-state DC holding circuit, there are a number of issues in meeting these requirements.

The Si3044 DC holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive DC feed, resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional way of dealing with this problem is to put a parallel RC shunt across the hookswitch relay. The capacitor is large (~1 uF, 250 V) and relatively expensive. In the Si3044, the OHS bit in Register 16 can be used to slowly ramp down the loop current to pass these tests without requiring additional components.

Billing Tone Detection

"Billing tones" or "metering pulses" generated by the central office can cause modem connection difficulties. The billing tone is typically either a 12 KHz or 16 KHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major errors related to the modem data. The Si3044 chipset has a feature which allows the device to provide feedback as to whether a billing tone has occurred and when it ends.

Billing tone detection is enabled by setting the BTE bit (Register 17, bit 2). Billing tones less than 1.1 V_{PK} on the line will be filtered out by the low pass digital filter on the Si3044. The ROV bit is set when a line signal is greater than 1.1 V_{PK}, indicating a receive overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the line-side device (Si3015).

When the BTD bit is set, the DC termination is changed to an 800 Ω DC impedance. This ensures minimum line voltage levels even in the presence of billing tones.

The OVL bit (Register 19) should be polled following a billing tone detection. When the OVL bit returns to zero, indicating that the billing tone has passed, the BTE bit should be written to zero to return the DC termination to its original state. It will take approximately one second to return to normal DC operating conditions. The BTD and ROV bits are sticky, and they must be written to zero to be reset. After the BTE, ROV, and BTD bits are all cleared, the BTE bit can be set to reenable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. The user should look for multiple events before qualifying whether billing tones are actually present.

Although the DAA will remain off-hook during a billing tone event, the received data from the line will be corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries/customers.

Alternatively, when a billing tone is detected, the system software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

Billing Tone Filter (Optional)

In order to operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. (The Si3044 can remain off-hook during a billing tone event, but modem data will be lost in the presence of large billing tone signals.) The notch filter design requires two notches, one at 12 KHz and one at 16 KHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 25 shows an example billing tone filter. Figure 26 shows the billing tone filter and the ringer impedance network for the Czech Republic. Both of these circuits may be combined into a single external dongle.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 KHz and 16 KHz.

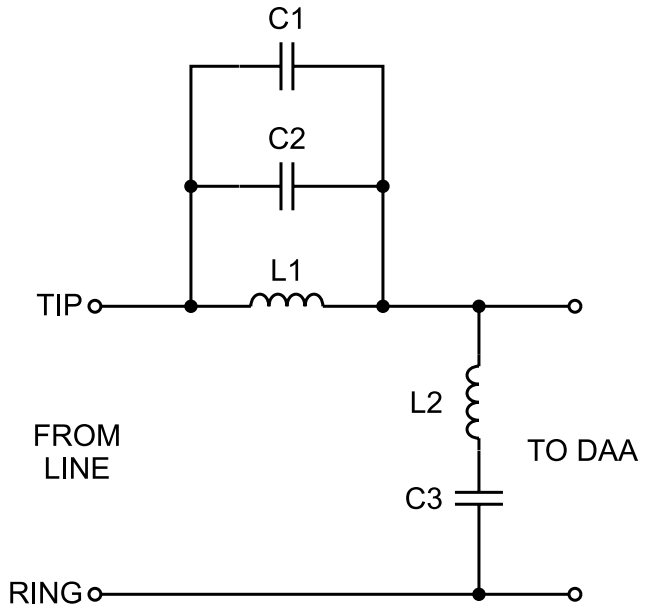


Figure 25. Billing Tone Filter

Table 20. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 µF, 50 V, ±10%
C3	0.01 µF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

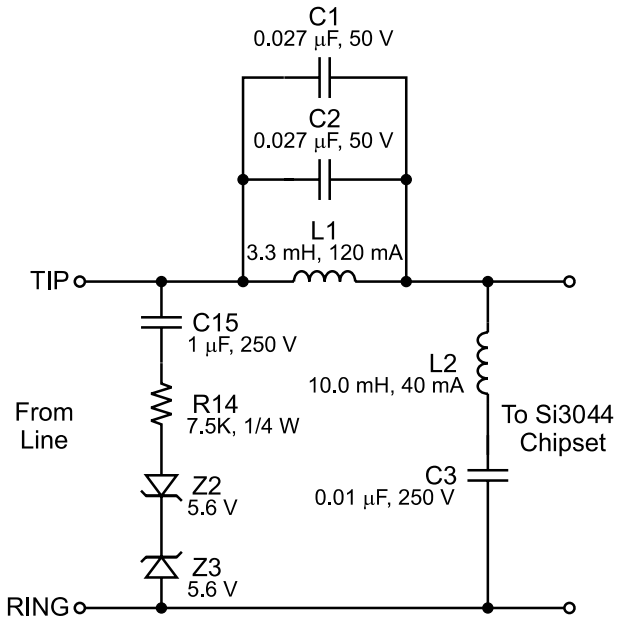


Figure 26. Dongle Applications Circuit

The billing tone filter affects the AC termination and return loss. The current complex AC termination will pass worldwide return loss specifications both with and without the billing tone filter by at least 3 dB. The AC termination is optimized for frequency response and hybrid cancellation, while having greater than 4 dB of margin with or without the dongle for South Africa, Australia, CTR21, German, and Swiss country-specific specifications.

On-Hook Line Monitor

The Si3044 allows the user to receive line activity when in an on-hook state. This is accomplished through a low-power ADC located on the line-side chip that digitizes the signal passed across the RNG1/2 pins and then sends this signal digitally across the ISOcap link to the DSP. This mode is typically used to detect caller ID data. (See the “Caller ID” section.) Note that there are two low-power ADCs on the Si3044. One is for backward compatibility with the Si3034, and is enabled by setting the ONHM bit in Register 5. This ADC draws approximately 450 µA of current from the line when activated. A new lower power ADC has been added to the Si3044, which enables a reduced current draw from the line of approximately 7 µA. This lower power ADC is enabled by setting the MODE bit (in conjunction with the ONHM bit) in Register 18 to 1. (See the MODE bit description for Register 18 in the “Control Registers” section.) Regardless of which ADC is being used, the on-hook line monitor function must be disabled before the device is taken off-hook. When using the OH bit, ensure that the ONHM bit is cleared before setting the OH bit. If using the hardware OFHK pin, ensure that the ONHM bit is cleared and one sample period has passed before driving the OFHK pin low.

The signal to the lower power ADC can be attenuated to accommodate larger signals. This is accomplished through the use of the ARX[2:0] bits in Register 15. It is important to note that while these ARX bits provide gain to the normal receive path of the DAA, they also function as attenuation bits for the on-hook line monitor low power ADC. Attenuation settings include 0 dB, 1 dB, 2.2 dB, 3.5 dB, and 5 dB. It is recommended that the new lower power ADC be used for on-hook line monitoring.

Caller ID

The Si3044 provides the designer with the ability to pass caller ID data from the phone line to a caller ID decoder connected to the serial port.

Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook.

In systems where the caller ID data is passed on the phone line between the first and second rings, the following method should be utilized to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in "Ring Detection" on page 25, determine when the first ring has completed.
2. If the Si3015 line-side device is revision D or higher (see the"Revision Identification" on page 36) then set the OFF/SQL2 bit (Register 16, bit 7). If the Si3015 line-side device is revision C or earlier, set the SQLH bit (Register 18, bit 0) for a period of at least 1 ms. These bits reset the AC coupling network on the ring input in preparation for the caller ID data.
3. If the SQLH bit was set, clear it after waiting at least 1 ms. If the OFF/SQL2 bit was set, it should not be cleared until after the caller ID data has been received.
4. Assert the MODE bit (Register 18, bit 2) and then the ONHM bit (Register 5, bit 3). This enables the lower current caller ID ADC.
5. The low-power ADC (which is powered from the system chip, allowing for approximately 7 µA current draw from the line) then digitizes the caller ID data passed across the RNG 1/2 pins and presents the data to the DSP via the SDO pin.
6. Clear the ONHM, MODE, and OFF/SQL2 (if used) bits after the caller ID data has been received but prior to the start of the second ring.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, the following method should be used to capture the caller ID data:

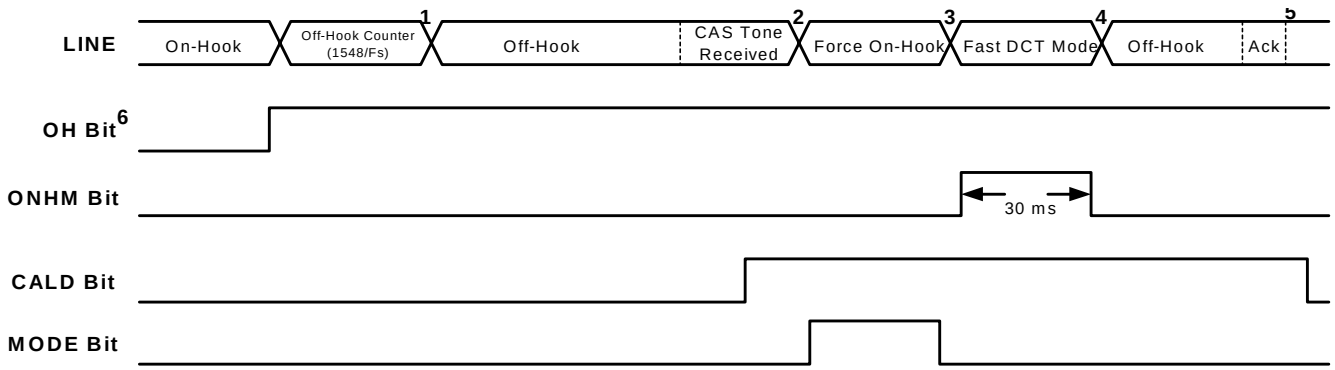
1. Enable full wave rectified ring detection (RFWE, Register 18, bit 1).
2. Monitor the RDTP and RDTN register bits to identify whether a polarity reversal or a ring signal has occurred. A polarity reversal will trip either the RDTP or RDTN ring detection bits, and thus the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Once the signal has been identified as a battery reversal, the AC coupling network on the ring input must be reset in preparation for the caller ID data. If the Si3015 line-side device is revision D or higher (see "Revision Identification" on page 36) then set the OFF/SLQ2 bit (Register 16, bit 7). If the Si3015 line-side device is revision C or earlier, set the SQLH bit (Register 18, bit 0) for a period of at least 1 ms.
4. If the SQLH bit was set, clear it after waiting at least 1 ms. If the OFF/SLQ2 bit was set, it should not be cleared until after the caller ID data has been received.
5. Assert the MODE bit (Register 18, bit 2) and then the ONHM bit (Register 5, bit 3). This enables the lower current caller ID ADC.
6. The low-power ADC (which is powered from the system chip, allowing for approximately 7 µA current draw from the line) then digitizes the caller ID data passed across the RNG 1/2 pins and presents the data to the DSP via the SDO pin.
7. Clear the ONHM, MODE, and OFF/SLQ2 (if used) bits after the caller ID data has been received but prior to the start of the second ring.

Type II Caller ID

Type II Caller ID sends the CID data while the phone is off-hook. This mode is often referred to as caller ID/ call waiting (CID/CW). To receive the CID data while off-hook, the following procedure should be used (also see Figure 27):

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The host processor must detect the presence of this tone.
2. The DAA must then check to see if there is another parallel device on the same line. This is accomplished by briefly going on-hook, measuring the line voltage, and then returning to an off-hook state.
   a. Set the CALD bit (Register 17, bit 5) to 1. This disables the calibration that automatically occurs when going off-hook.
   b. With the OH bit (Register 5, bit 0) set to 1 and the ONHM bit (Register 5, bit 3) set to 0, set the MODE bit (Register 18, bit 2) to 1. This forces the DAA to go on-hook and disables the off-hook counter that is normally enabled when going back off-hook.
   c. Read the LVCS bits to determine the state of the line.
   d. If the LVCS bits read the typical on-hook line voltage, then there are no parallel devices active on the line, and CID data reception can be continued.
   e. If the LVCS bits read well below the typical on-hook line voltage, then there are one or more devices present and active on the same line that are not compliant with Type II CID. CID data reception should not be continued.
   f. Set the MODE bit to 0 to return to an off-hook state.
3. Immediately after returning to an off-hook state, the ONHM bit must be set and left enabled for at least 30 ms. This allows the line voltage to settle before transmitting or receiving any data. After 30 ms, the ONHM bit should be disabled to allow normal data transmission and reception.
4. If a non-compliant parallel device is present, then a reply tone is not sent by the host tone generator and the CO does not proceed with sending the CID data.
5. If all devices on the line are Type II CID compliant, then the host must mute its upstream data output to avoid the propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the host processor must then send an acknowledgement (ACK) tone back to the CO to request the transmission of the CID data.
6. The CO then responds with the CID data. After receiving this, the host processor unmutes the upstream data output and continues with normal operation.
7. The muting of the upstream data path by the host processor has the effect of muting the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.
8. The CALD bit can be set to 0 to re-enable the automatic calibration when going off-hook.

Due to the nature of the low-power ADC, the data presented on SDO could have up to a 10% DC offset. The caller ID decoder must either use a high pass or a band pass filter to accurately retrieve the caller ID data.



Notes:

1. The off-hook counter is used to prevent transmission or reception of data for 1548/Fs to allow time for the line voltage to settle. If the CALD bit is 0, an automatic calibration will also be performed during this time.
2. The caller alert signal (CAS) tone is transmitted from the CO, which signals an incoming call.
3. When the MODE bit is set while the device is off-hook, the device is forced on-hook. This is done to read the line voltage in the LVCS bits to detect parallel handsets. In this mode, no data is transmitted on the SDO pin.
4. When the device returns off-hook after being forced on-hook using the MODE bit, the normal off-hook counter is disabled. Additionally, if the CALD bit is set, the automatic calibration will not be performed. The fast DCT mode must be manually enabled for at least 30 ms in order to properly settle the line voltage. This is done by setting the ONHM bit after disabling the MODE bit.
5. After allowing the line voltage to settle in fast DCT mode, normal off-hook mode should be entered by disabling the ONHM bit. If CID data reception is desired, then the appropriate signal should be sent to the CO at this time.
6. This example uses the OH bit to put the Si3044 into an off-hook state. The $\overline{\text{OFHK}}$ pin may also be used to accomplish this. To use the $\overline{\text{OFHK}}$ pin instead of the OH bit, simply enable the OHE bit (Register 5, bit 1) and drive the $\overline{\text{OFHK}}$ pin low during the above sequence. This has the same effect as setting the OH bit.

Figure 27. Implementing Type II Caller ID on the Si3044

Overload Protection

The Si3044 can detect if an overload condition is present which may damage the DAA circuit. The DAA may be damaged if excessive line voltage or loop current is sustained.

The overload protection circuit utilizes the LVCS bits to determine an excessive line current or voltage per the LVCS bit transfer functions outlined in Figures 18 and 19.

When off-hook, if OPE is set and LVCS = 11111, the DC termination is disabled (800 Ω presented to the line), the hookswitch current is reduced, and the OPD bit (Register 19) is set.

Note: If the OPE bit is enabled before going off-hook, the overload protection circuit could be activated by the line transients produced by going off-hook. To avoid this, the OPE bit should be 0 prior to going off-hook. This bit can then be set ~25 ms after going off-hook to enable the overload protection feature.

Analog Output

The Si3044 supports an analog output (AOUT) for driving the call progress speaker found with most of today's modems. AOUT is an analog signal that is comprised of a mix of the transmit and receive signals. The receive portion of this mixed signal has a 0 dB gain, while the transmit signal has a gain of –20 dB.

The transmit and receive signals of the AOUT signal have independent controls found in Register 6. The ATM[1:0] bits control the transmit portion, while the ARM[1:0] bits control the receive portion. Note that the bits only affect the AOUT signal and do not affect the modem data. Figure 17 on page 18 illustrates a recommended application circuit. Note that in the configuration shown, the LM386 provides a gain of 26 dB. Additional gain adjustments may be made by varying the voltage divider created by R1 and R3.

Gain Control

The Si3044 supports multiple receive gain and transmit attenuation settings in Register 15. The receive path can support gains of 0, 3, 6, 9, and 12 dB, as selected with the ARX[2:0] bits. The receive path can also be muted with the RXM bit. The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB, as selected with the ATX[2:0] bits. The transmit path can also be muted with the TXM bit.

The gain control bits ARXB and ATXB in Register 13 are provided for firmware backwards compatibility with the Si3032 and Si3035 chipsets. These bits should be set to zero if the ARX[2:0] and ATX[2:0] in Register 15 are used.

Filter Selection

The Si3021 supports additional filter selections for the receive and transmit signals as defined in Table 11 and Table 12 on page 12. The IIRE bit in Register 16 selects between the IIR and FIR filters. The IIR filter provides a lower, but non-linear, group delay than the default FIR filter.

Clock Generation Subsystem

The Si3044 contains an on-chip clock generator. Using a single MCLK input frequency, the Si3044 can generate all the desired standard modem sample rates, as well as the common 11.025 kHz rate for audio playback.

The clock generator consists of two phase-locked loops (PLL1 and PLL2) that achieve the desired sample frequencies. Figure 28 illustrates the clock generator. The architecture of the dual PLL scheme allows for fast lock time on initial start-up, fast lock time when changing modem sample rates, high noise immunity, and the ability to change modem sample rates with a single register write. A large number of MCLK frequencies between 1 MHz and 60 MHz are supported. MCLK should be from a clean source, preferably directly from a crystal with a constant frequency and no dropped pulses.

In serial mode 2, the Si3021 operates as a slave device. The clock generator is configured (by default) to set the SCLK output equal to the MCLK input. The net effect is the clock generator multiplies the MCLK input by 20. For further details of slave mode operation, refer to "Multiple Device Support" on page 34.

Programming the Clock Generator

As noted in Figure 28, the clock generator must output a clock equal to 1024*Fs, where Fs is the desired sample rate. The 1024*Fs clock is determined through programming of the following registers:

- Register 7: PLL1 N1[7:0] divider.
- Register 8: PLL1 M1[7:0] divider.
- Register 9: PLL2 N2[3:0] and M2[3:0] dividers.
- Register 10: CGM Clock Generation Mode.

The main design consideration is the generation of a base frequency, defined as follows:

$$F_{BASE} = \frac{F_{MCLK} \cdot M1}{N1} = 36.864MHz \text{ CGM=0}$$

$$F_{BASE} = \frac{F_{MCLK} \cdot M1 \cdot 16}{N1 \cdot 25} = 36.864MHz \text{ CGM=1}$$

N1 (Register 7) and M1 (Register 8) are 8-bit unsigned values. F_{MCLK} is the frequency of the clock provided to the MCLK pin. Table 21 lists several standard crystal oscillator rates that could be supplied to MCLK. This list simply represents a sample of MCLK frequency choices. Many more are possible.

After PLL1 and the CGM bit have been programmed, PLL2 can be used to achieve all of the standard modem sampling rates with a single write to Register 9. These standard sample rates are shown in Table 22. The values for N2 and M2 (Register 9) are shown in Table 22. N2 and M2 are 4-bit unsigned values.

When programming the registers of the clock generator, the order of register writes is important. For PLL1 updates, N1 (Register 7) must always be written first, immediately followed by a write to M1 (Register 8). For PLL2, the CGM bit must set as desired prior to writing N2 and M2 (Register 9). Changes to CGM only take effect when N2 and M2 are written.

The values shown in Table 21 and Table 22 satisfy the equations above. However, when programming the registers for N1, M1, N2, and M2, the value placed in these registers must be one less than the value calculated from the equations. For example, for CGM = 0 with an MCLK of 48.0 MHz, the values placed in the N1 and M1 registers would be 7Ch and 5Fh, respectively. If CGM = 1, a non-zero value must be programmed to Register 9 in order for the 16/25 ratio to take effect.

PLL Lock Times

The Si3044 changes sample rates very quickly. However, lock time will vary based on the programming of the clock generator. The major factor contributing to PLL lock time is the CGM bit. When the CGM bit is used (set to one), PLL2 will lock slower than when CGM is zero. The following relationships describe the boundaries on PLL locking time:

PLL1 lock time < 1 ms (CGM = 0,1)
PLL2 lock time 100 µs to 1 ms (CGM = 0)
PLL2 lock time <1 ms (CGM = 1)

For modem designs, it is recommended that PLL1 be programmed during initialization. No further programming of PLL1 is necessary. The CGM bit and PLL2 can be programmed for the desired initial sample rate, typically 7200 Hz. All further sample rate changes are made by simply writing to Register 9 to update PLL2.

The final design consideration for the clock generator is the update rate of PLL1. The following criteria must be satisfied in order for the PLLs to remain stable:

$$F_{UP1} = \frac{F_{MCLK}}{N1} \geq 144KHz$$

where F_{UP1} is shown in Figure 28.

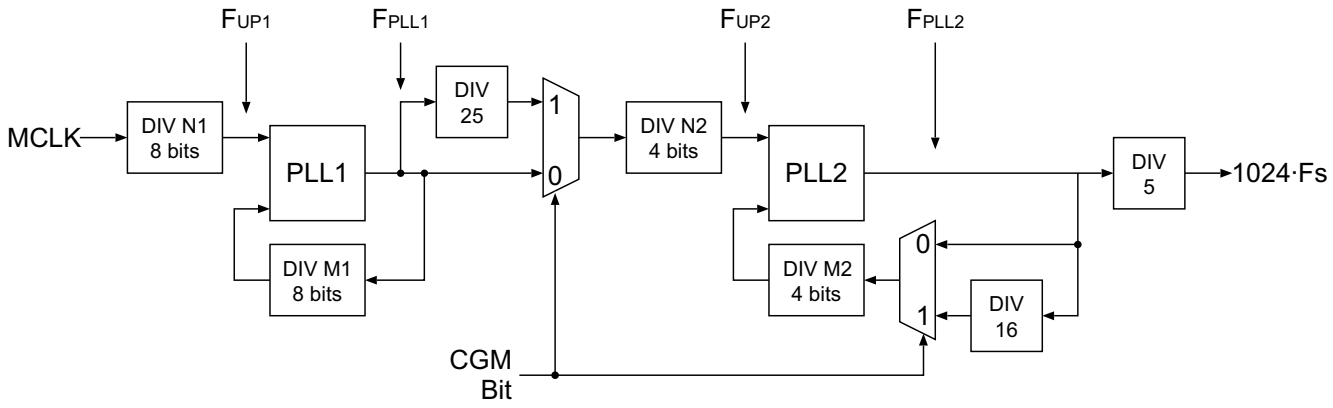


Figure 28. Clock Generation Subsystem

Table 21. MCLK Examples

MCLK (MHz)	N1	M1	CGM
1.8432	1	20	0
4.0000	5	72	1
4.0960	1	9	0
5.0688	11	80	0
6.0000	5	48	1
6.1440	1	6	0
8.1920	32	225	1
9.2160	1	4	0
10.0000	25	144	1
10.3680	9	32	0
11.0592	3	10	0
12.288	1	3	0
14.7456	2	5	0
16.0000	5	18	1
18.4320	1	2	0
24.5760	2	3	0
25.8048	7	10	0
33.8688	147	160	0
44.2368	96	125	1

Table 21. MCLK Examples

MCLK (MHz)	N1	M1	CGM
46.0800	5	4	0
47.9232	13	10	0
48.0000	125	96	0
56.0000	35	36	1
60.0000	25	24	1

Table 22. N2, M2 Values (CGM = 0,1)

Fs (Hz)	N2	M2
7200	2	2
8000	9	10
8229	7	8
8400	6	7
9000	4	5
9600	3	4
10286	7	10

Setting Generic Sample Rates

The clock generation description focuses on the common modem sample rates. An application may require a sample rate not listed in Table 22, such as the common audio rate of 11.025 kHz. The restrictions and equations above still apply; however, a more generic relationship between MCLK and Fs (the desired sample rate) is needed. The following equation describes this relationship:

$$\frac{M1 \bullet M2}{N1 \bullet N2} = ratio \bullet \frac{5 \bullet 1024 \bullet Fs}{MCLK}$$

where Fs is the sample frequency, ratio = 1 for CGM = 0 and ratio = 25/16 for CGM = 1. All other symbols are shown in Figure 28.

By knowing the MCLK frequency and desired sample rate, the values for the M1, N1, M2, N2 registers can be determined. When determining these values, remember to consider the range for each register as well as the minimum update rate for the first PLL.

The values determined for M1, N1, M2, and N2 must be adjusted by –1 when determining the value written to the respective registers. This is due to internal logic, which adds one to the value stored in the register. This addition allows the user to write a zero value in any of the registers and the effective divide by is one. A special case occurs when both M1 and N1 and/or M2 and N2 are programmed with a zero value. When Mx and Nx are both zero, the corresponding PLLx is bypassed. Note that if M2 and N2 are set to zero, the ratio of 25/16 is eliminated and cannot be used in the above equation. In this condition the CGM bit has no effect.

Digital Interface

The Si3044 has two serial interface modes that support most standard modem DSPs. The M0 and M1 mode pins select the interface mode. The key difference between these two serial modes is the operation of the $\overline{\text{FSYNC}}$ signal. Table 23 summarizes the serial mode definitions.

Table 23. Serial Modes

Mode	M1	M0	Description
0	0	0	$\overline{\text{FSYNC}}$ frames data
1	0	1	$\overline{\text{FSYNC}}$ pulse starts data frame
2	1	0	Slave mode
3	1	1	Reserved

The digital interface consists of a single, synchronous serial link which communicates both telephony and control data.

In Serial mode 0 or 1, the Si3021 operates as a master, where the master clock (MCLK) is an input, the serial data clock (SCLK) is an output, and the frame sync signal ($\overline{\text{FSYNC}}$) is an output. The MCLK frequency and the value of the sample rate control registers 7, 8, 9 and 10 determine the sample rate (Fs). The serial port clock, SCLK, runs at 256 bits per frame, where the frame rate is equivalent to the sample rate. Refer to "Clock Generation Subsystem" on page 31 for more details on programming sample rates.

The Si3044 transfers 16-bit or 15-bit telephony data in the primary timeslot and 16-bit control data in the secondary timeslot. Figure 29 and Figure 30 show the relative timing of the serial frames. Primary frames occur at the frame rate and are always present. To minimize overhead in the external DSP, secondary frames are present only when requested.

Two methods exist for requesting a secondary frame to transfer control information. The default power-up mode uses the LSB of the 16-bit transmit (TX) data word as a flag to request a secondary transfer. In this mode, only 15-bit TX data is transferred, resulting in a loss of SNR but allowing software control of the secondary frames. As an alternative method, the FC pin can serve as a hardware flag for requesting a secondary frame. The external DSP can turn on the 16-bit TX mode by setting the SB bit in Register 1. In the 16-bit TX mode, the hardware FC pin must be used to request secondary transfers.

Figure 31 and Figure 32 illustrate the secondary frame read cycle and write cycle, respectively. During a read cycle, the R/$\overline{\text{W}}$ bit is high and the 5-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed on the SDO signal. During a write cycle, the R/$\overline{\text{W}}$ bit is low and

the 5-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on SDI. Only one register can be read or written during each secondary frame. See "Control Registers" on page 44 for the register addresses and functions.

In serial mode 2, the Si3021 operates as a slave device, where MCLK is an input, SCLK is a no connect, and FSYNC is an input. In addition, the RGDT/FSD pin operates as a delayed frame sync (FSD) and the FC/RGDT pin operates as ring detect (RGDT). Note that in this mode, FC operation is not supported. For further details on operating the Si3021 as a slave device, refer to “Multiple Device Support”.

Multiple Device Support

The Si3044 supports the operation of up to 7 additional devices on a single serial interface. Figure 37 shows the typical connection of the Si3044 and one additional serial voice codec (Si3000).

The Si3044 must be the master in this configuration. The secondary codec should be configured as a slave device with the master’s SCLK used as the MCLK input to the codec, and the master’s frame sync delay signal (FSD) used as the codec’s FSYNC input. On power up, the Si3044 master will be unaware of the additional codec on the serial bus. The FC/RGDT pin is an input, operating as the hardware control for secondary frames, and the RGDT/FSD pin is an output, operating as the active low ring detection signal. The master device should be programmed for master/slave mode prior to enabling the ISOcap link, because a ring signal would cause a false transition to the slave device’s FSYNC.

Register 14 provides the necessary control bits to configure the Si3044 for master/slave operation. Bit 0 (DCE) sets the Si3044 in master/slave mode, also referred to as daisy-chain mode. When the DCE bit is set, the FC/RGDT pin becomes the ring detect output and the RGDT/FSD pin becomes the frame sync delay output. When using multiple devices, secondary frame communication must be requested via software in the LSB of the transmit (TX) data word.

Bits 7:5 (NSLV2:NSLV0) set the number of slaves to be supported on the serial bus. For each slave, the Si3044 will generate an FSYNC to the DSP. In daisy-chain mode, the polarity of the ring signal can be controlled by bit 1 (RPOL). When RPOL = 1, the ring detect signal (now an output on the FC/RGDT pin) is active high.

The Si3044 supports a variety of codecs as well as additional Si3044s. The type of slave codec(s) used is set by bits 4:3 (SSEL1:SSEL0). These bits determine the type of signalling used in the LSB of SDO. This assists the DSP in isolating which data stream is the master and which is the slave. If the LSB is used for signalling, the master device will have a unique setting relative to the slave devices. The DSP can use this information to determine which FSYNC marks the beginning of a sequence of data transfers.

The delayed frame sync (FSD) of each device is supplied as the FSYNC of each subsequent slave device in the daisy chain. The master Si3044 will generate an FSYNC signal for each device every 16 or 32 SLCK periods. The delay period is set by Register 14, bit 2 (FSD). Figures 33–36 show the relative timing for daisy chaining operation. Note that primary communication frames occur in sequence, followed by secondary communication frames, if requested. When writing/reading the master device via a secondary frame, all secondary frames of the slave devices must be written as well. When writing/reading a slave device via a secondary frame, the secondary frames of the master and all other slaves must be written as well. "No operation" writes/reads to secondary frames are accomplished by writing/reading a zero value to address zero.

If FSD is set for 16 SCLK periods between FSYNCs, only serial mode 1 can be used. In addition, the slave devices must delay the tri-state to active transition of their SDO sufficiently from the rising edge of SCLK to avoid bus contention.

The Si3044 supports the operation of up to eight Si3044 devices on a single serial bus. The master Si3044 must be configured in serial mode 1. The slave(s) Si3044 should be configured in serial mode 2. Figure 38 on page 43 shows a typical master/slave connection using three Si3044 devices.

When in serial mode 2, FSYNC becomes an input, RGDT/FSD becomes the delay frame sync output, and FC/RGDT becomes the ring detection output. In addition, the internal PLLs are fixed to a multiply by 20. This provides the desired sample rate when the master’s SCLK is provided to the slave’s MCLK. Note that the SCLK of the slave is a no connect in this configuration.

The delay between FSYNC input and delayed frame sync output (RGDT/FSD) will be 16 SCLK periods. The RGDT/FSD output has a waveform identical to the FSYNC signal in serial mode 0. In addition, the LSB of SDO is set to zero by default for all devices in serial mode 2.

Power Management

The Si3044 supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full power down mode. The power management modes are controlled by the PDN and PDL bits in Register 6.

On power up, or following a reset, the Si3044 is in reset operation. In this mode, the PDL bit is set, while the

PDN bit is cleared. The Si3021 is fully operational, except for the ISOcap link. No communication between the Si3021 and Si3015 can occur during reset operation. Note that any bits associated with the Si3015 are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The Si3021 is fully operational and the ISOcap link is passing information between the Si3021 and the Si3015. Note that the clock generator must be programmed to a valid sample rate prior to entering this mode.

The Si3044 supports a low-power sleep mode. This mode supports the popular wake-up-on-ring feature of many modems. The clock generator registers 7, 8, and 9 must be programmed with valid non-zero values prior to enabling sleep mode. The PDN bit must then be set and the PDL bit cleared. When the Si3044 is in sleep mode, the MCLK signal may be stopped or remain active, but it *must* be active before waking up the Si3044. The Si3021 is non-functional except for the ISOcap link and the RGDT signal. To take the Si3044 out of sleep mode, pulse the reset pin (RESET) low.

In summary, the power down/up sequence for sleep mode is as follows:

1. Registers 7, 8, and 9 must have valid non-zero values.
2. Set the PDN bit (Register 6, bit 3) and clear the PDL bit (Register 6, bit 4).
3. MCLK may stay active or stop.
4. Restore MCLK before initiating the power-up sequence.
5. Reset the Si3044 by pulsing the RESET pin (after MCLK is present).
6. Program registers to desired settings.

The Si3044 also supports an additional power-down mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) bits are set, the chipset enters a complete power-down mode and draws negligible current (deep sleep mode). PLL2 should be turned off prior to entering deep sleep mode (i.e., set Register 9 to 0 and then Register 6 to 18h). In this mode, the RGDT pin does not function. Normal operation may be restored using the same process for taking the chipset out of sleep mode.

Calibration

The Si3044 initiates an auto-calibration by default whenever the device goes off-hook or experiences a loss in line power. Calibration is used to remove any offsets that may be present in the on-chip A/D converter which could affect the A/D dynamic range. Auto-calibration is typically initiated after the DAA DC termination stabilizes, and takes 512/Fs seconds to complete. Due to the large variation in line conditions and line card behavior that can be presented to the DAA, it may be beneficial to use manual calibration in lieu of auto-calibration.

Manual calibration should be executed as close to 512/Fs seconds as possible before valid transmit/receive data is expected.

The following steps should be taken to implement manual calibration:

1. The CALD (auto-calibration disable—Register 17) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to one and then zero to begin and complete the calibration.
3. The calibration will be completed in 512/Fs seconds.

In-Circuit Testing

The Si3044's advanced design provides the designer with an increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Four loopback modes exist allowing increased coverage of system components. For three of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 1 on page 5 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side chip.

For the start-up test mode, no line-side power is necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line side is in a power-down mode and the DSP side is in a digital loop-back mode. In this mode, data received on SDI is passed through the internal filters and transmitted on SDO. This path will introduce approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters will exist between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line side. When the PDL bit is cleared the FDT bit (Register 12, bit 6) will become active, indicating the successful communication between the line side and DSP side. This can be used to verify that the ISOcap link is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirements:

1. Power up or reset.
2. Program clock generator to desired sample rate.
3. Enable line side by clearing PDL bit.
4. Issue off-hook

5. Delay 1548/Fs sec to allow calibration to occur.
6. Set desired test mode.

The ISOcap digital loopback mode allows the data pump to provide a digital input test pattern on SDI and receive that digital test pattern back on SDO. To enable this mode, set the DL bit in Register 1. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitor, C1 of Figure 16 on page 15, to the line side device and returned across the same barrier. Note in this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive a signal on the telephone line into the Si3015 line-side device and have it driven back out onto the line. This mode allows testing of external components connecting the RJ-11 jack (TIP and RING) to the Si3015. To enable this mode, set the AL bit in Register 2.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit and receive paths on the line-side chip and the external components in Figure 16 on page 15. In this test mode, the data pump provides a digital test waveform on SDI. This data is passed across the isolation barrier, transmitted to and received from the line, passed back across the isolation barrier, and presented to the data pump on SDO. To enable this mode, clear the HBE bit in Register 2.

When the HBE bit is cleared, this will cause a DC offset which affects the signal swing of the transmit signal. In this test mode, it is recommended that the transmit signal be 12 dB lower than normal transmit levels. This lower level will eliminate clipping caused by the DC offset which results from disabling the hybrid. It is assumed in this test that the line AC impedance is nominally 600 Ω.

Note: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

Exception Handling

The Si3044 provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit (FDT, Register 12 bit 6). This bit indicates that the DSP side (Si3021) and line-side (Si3015) devices are communicating. During normal operation, the FDT bit can be checked before reading any bits that indicate information about the line side. If FDT is not set, the following bits related to the line side are invalid—RDT, RDTN, RDTP, LCS[3:0], CBID, REVB[3:0], LVCS[4:0], ROV, BTD, DOD, OPD, and OVL; the $\overline{\text{RGDT}}$ operation will also be non-functional.

Following power-up and reset, the FDT bit is not set because the PDL bit (Register 6 bit 4) defaults to 1. In this state, the ISOcap is not operating and no information about the line side can be determined. The user must program the clock generator to a valid configuration for the system and clear the PDL bit to activate the ISOcap link. While the DSP and line side are establishing communication, the DSP side does not generate $\overline{\text{FSYNC}}$ signals. Establishing communication will take less than 10 ms. Therefore, if the controlling DSP serial interface is interrupt driven based on the $\overline{\text{FSYNC}}$ signal, the controlling DSP does not require a special delay loop to wait for this event to complete.

The FDT bit can also indicate if the line side executes an off-hook request successfully. If the line side is not connected to a phone line (that is, the user fails to connect a phone line to the modem), the FDT bit remains cleared. The controlling DSP must allow sufficient time for the line side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT bit is high, the LVCS[4:0] bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit in Register 6 must be set high for at least 1 ms to reset the line side.

Another useful bit is the communication link error (CLE) bit (Register 12, bit 7). The CLE bit indicates a time-out error for the ISOcap link following a change to either PLL1 or PLL2. When the CLE bit is set, the DSP-side chip has failed to receive verification from the line-side chip that the clock change has been accepted in an expected period of time (less than 10 ms). This condition indicates a severe error in programming the clock generator or possibly a defective line-side chip.

Revision Identification

The Si3044 provides the system designer the ability to determine the revision of the Si3021 and/or the Si3015. The REVA[3:0] bits in Register 11 identify the revision of the Si3021. The REVB[3:0] and CBID bits in Register 13 identify the revision of the Si3015. Table 24 lists revision values for both chips and may contain future revisions not yet in existence.

Table 24. Revision Values

Revision	Si3021	Si3015
C	1010	1011
D		1100

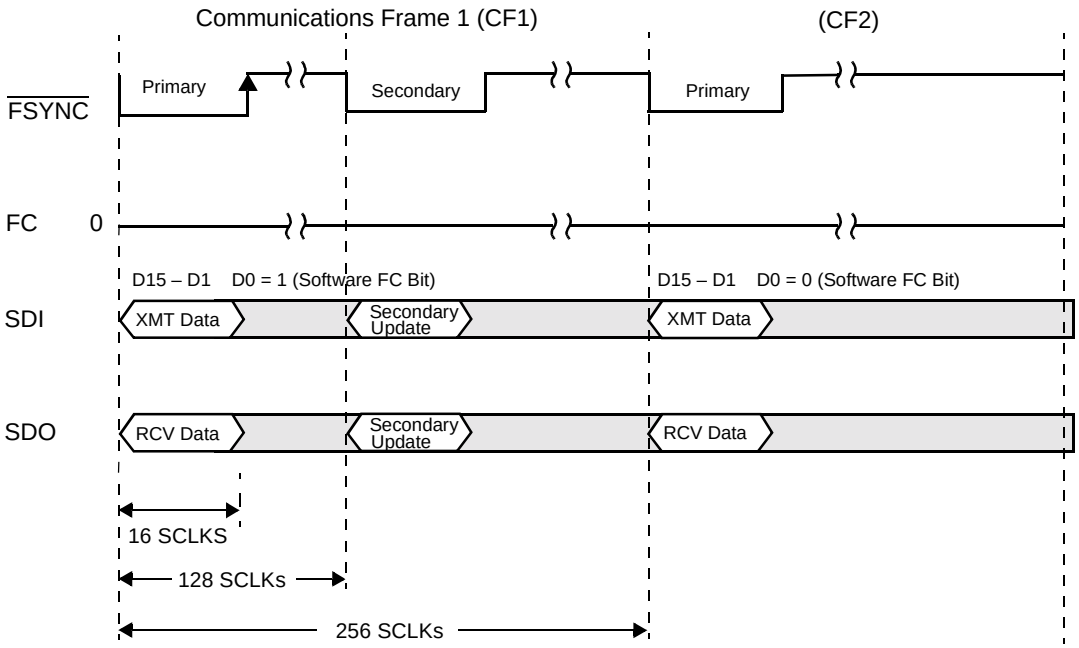


Figure 29. Software FC/$\overline{\text{RGDT}}$ Secondary Request

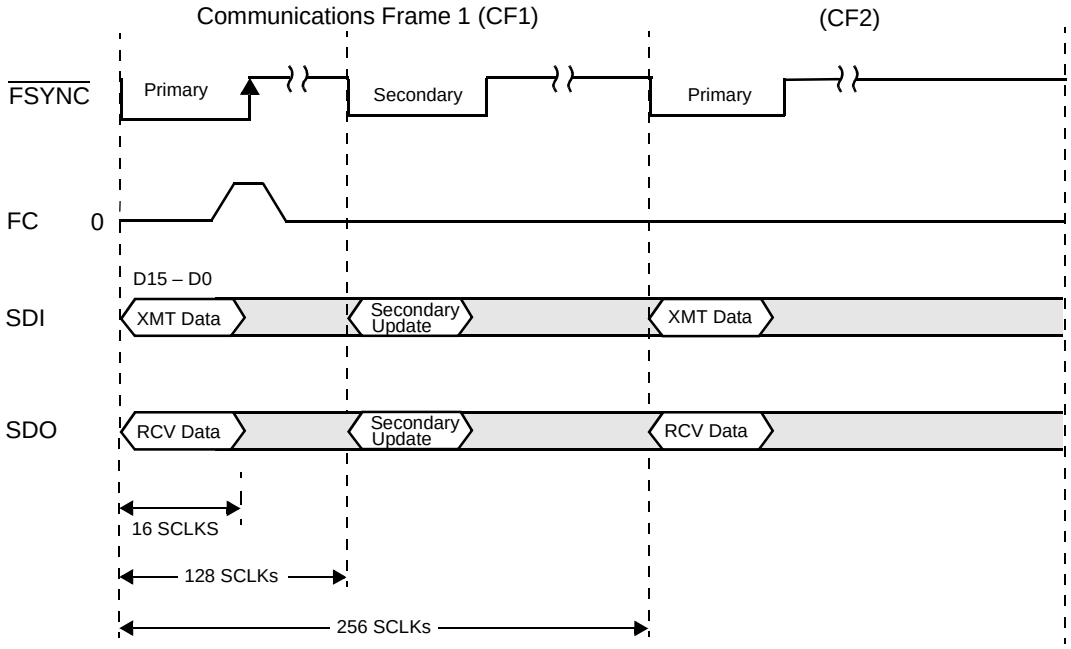


Figure 30. Hardware FC/$\overline{\text{RGDT}}$ Secondary Request

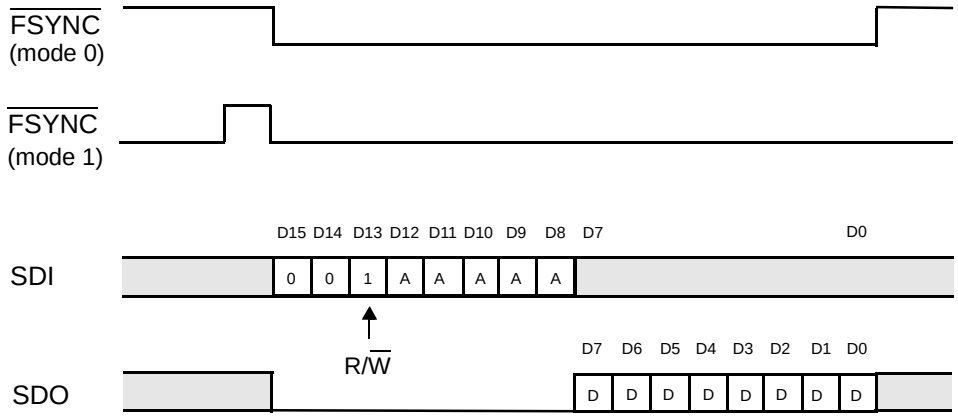


Figure 31. Secondary Communication Data Format—Read Cycle

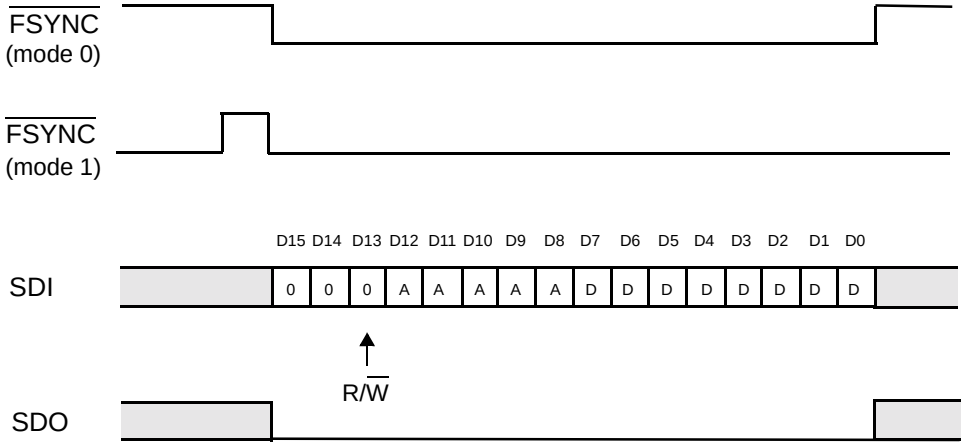


Figure 32. Secondary Communication Data Format—Write Cycle

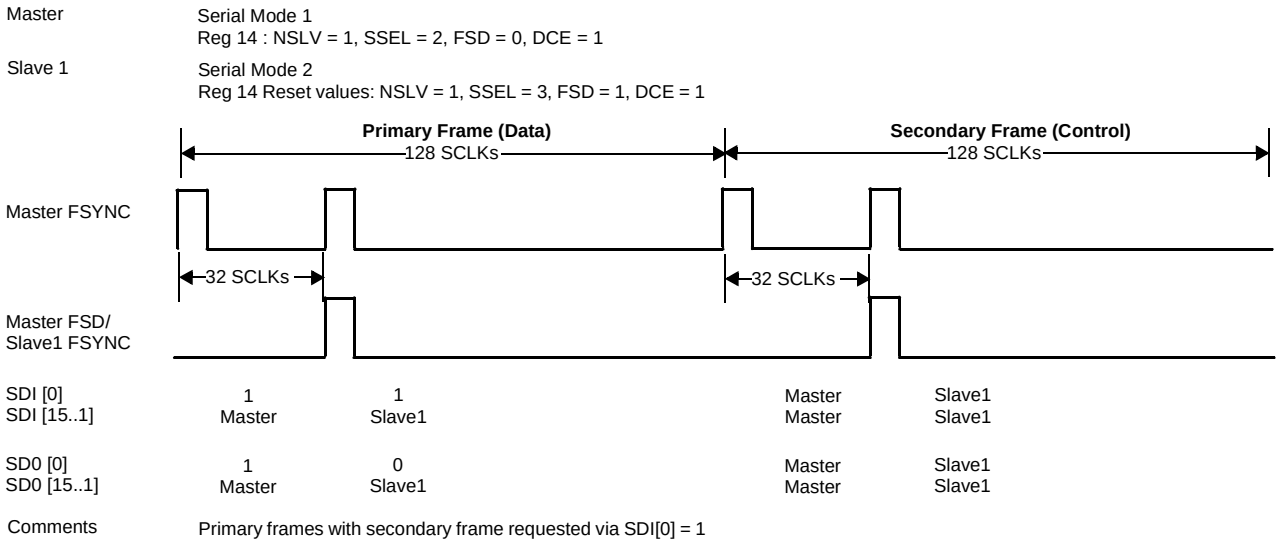


Figure 33. Daisy Chaining of a Single Slave (Pulse FSD)

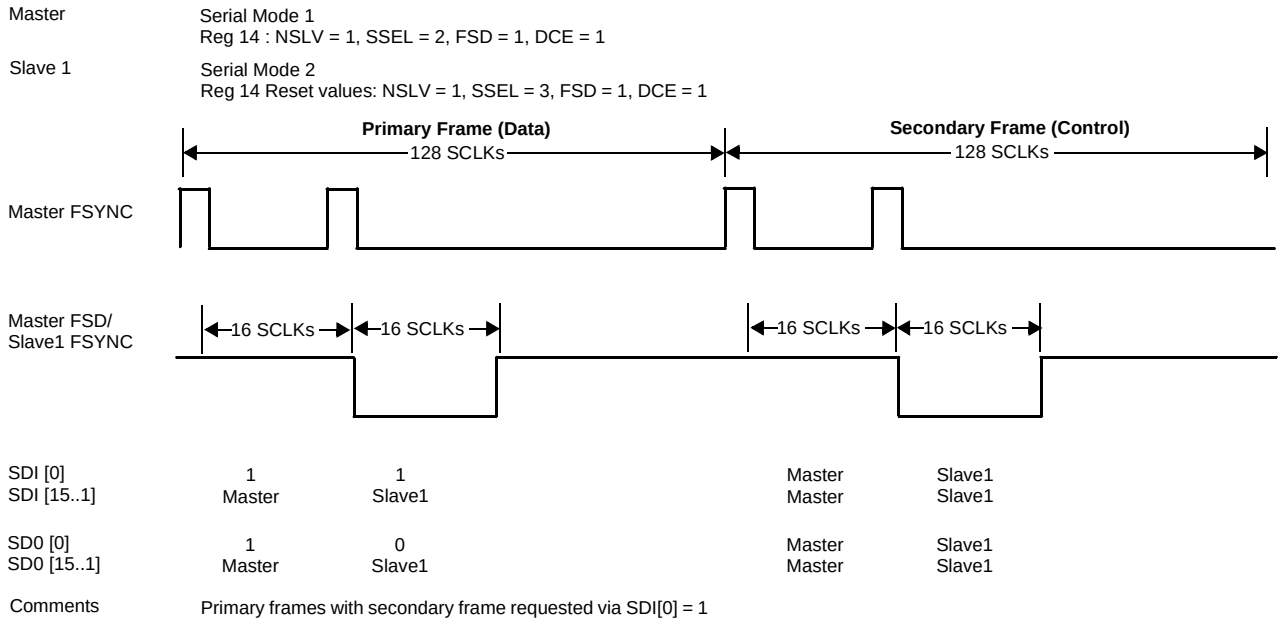


Figure 34. Daisy Chaining of a Single Slave (Frame FSD)

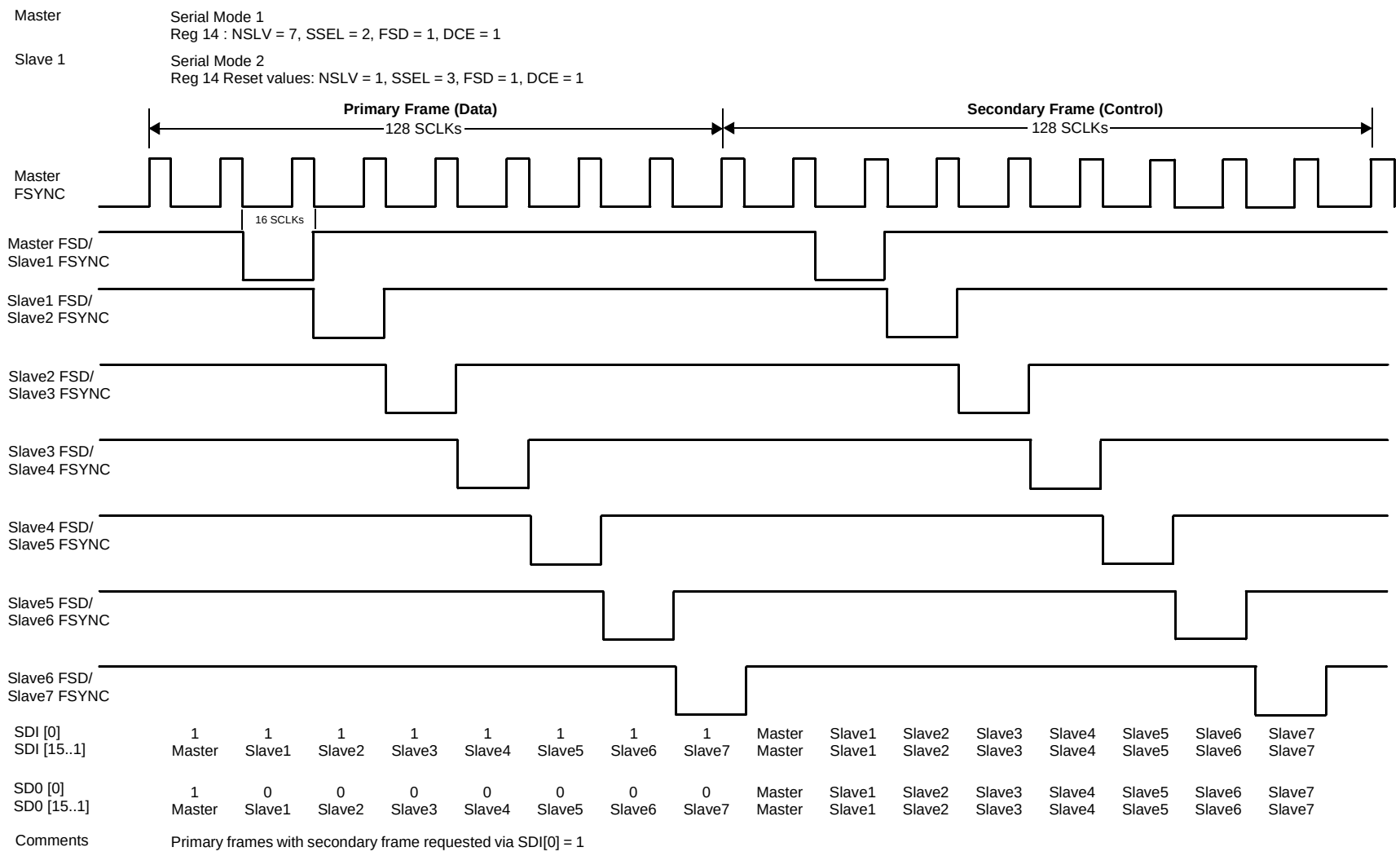


Figure 35. Daisy Chaining of Eight DAAs

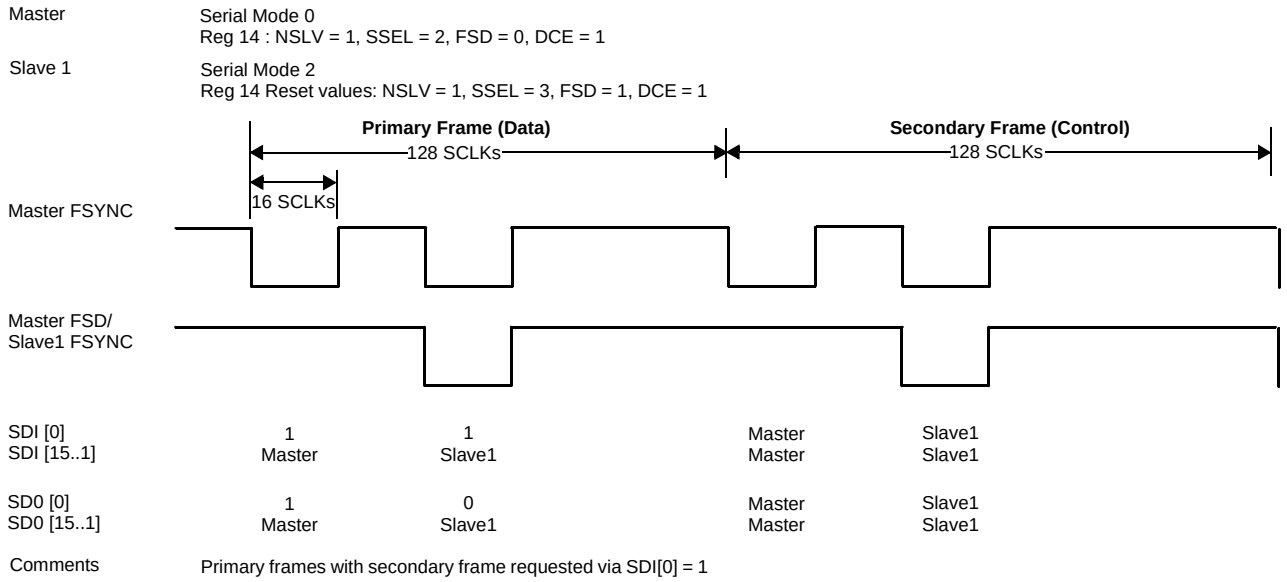


Figure 36. Daisy Chaining with Framed FSYNC and Framed FSD

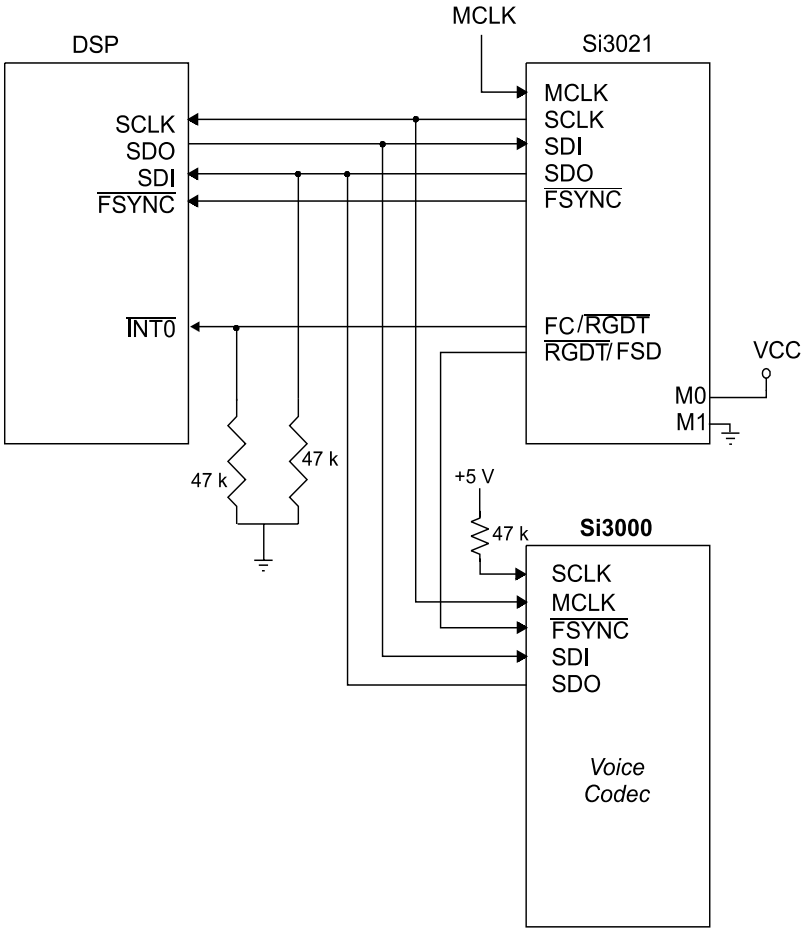


Figure 37. Typical Connection for Master/Slave Operation (e.g., Data/Fax/Voice Modem)

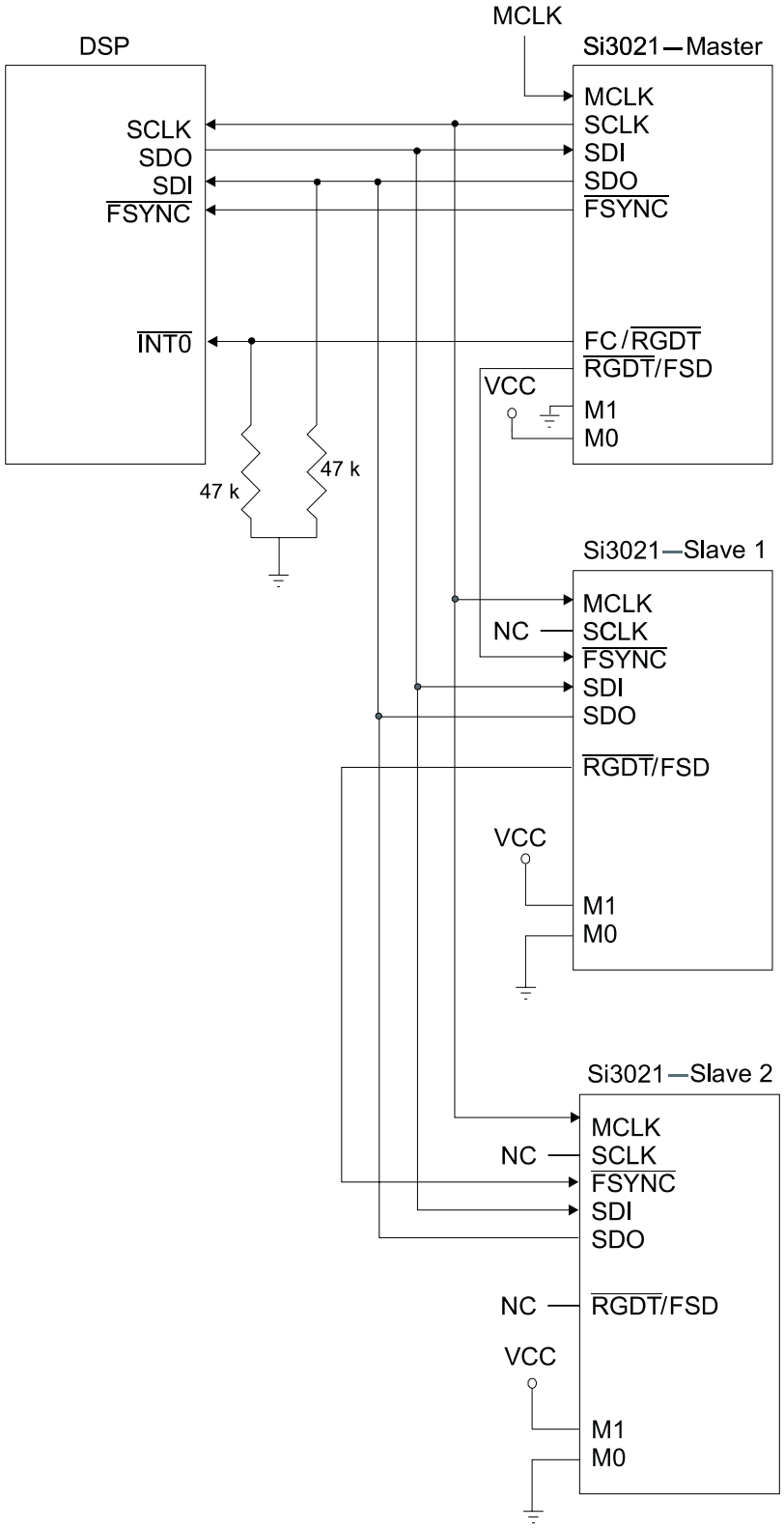


Figure 38. Typical Connection for Multiple Si3044s

Control Registers

Note: Any register not listed here is reserved and must not be written.

Table 25. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR						DL	SB
2	Control 2					AL		HBE	RXE
3	Reserved								
4	Reserved								
5	DAA Control 1		RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
6	DAA Control 2	CPE	ATM[1]	ARM[1]	PDL	PDN		ATM[0]	ARM[0]
7	PLL1 Divide N1	N1[7:0]							
8	PLL1 Divide M1	M1[7:0]							
9	PLL2 Divide N2/M2	N2[3:0]				M2[3:0]			
10	PLL Control								CGM
11	Chip A Revision					REVA[3:0]			
12	Line Side Status	CLE	FDT			LCS[3:0]			
13	Chip B Revision		CBID	REVB[3:0]				ARXB	ATXB
14	Daisy Chain Control	NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
15	TX/RX Gain Control	TXM	ATX[2:0]			RXM	ARX[2:0]		
16	International Control 1	OFF/ SQL2	OHS	ACT	IIRE	DCT[1:0]		RZ	RT
17	International Control 2		MCAL	CALD	LIM	OPE	BTE	ROV	BTD
18	International Control 3	FULL	DIAL	FJM	VOL	FLVM	MODE	RFWE	SQLH
19	International Control 4	LVCS[4:0]					OVL	DOD	OPD

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR						DL	SB
Type	R/W						R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset.** 0 = Enables the chip for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit will automatically clear after being set.
6:2	Reserved	Read returns zero.
1	DL	**Isolation Digital Loopback.** 0 = Digital loopback across the isolation barrier is disabled. 1 = Enables digital loopback mode across the isolation barrier. The line side must be enabled prior to setting this mode.
0	SB	**Serial Digital Interface Mode.** 0 = Operation is in 15-bit mode, and the LSB of the data field indicates whether a secondary frame is required. 1 = The serial port is operating in 16-bit mode and requires use of the secondary frame sync signal, FC, to initiate control data reads/writes.

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					AL		HBE	RXE
Type					R/W		R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	AL	**Analog Loopback.** 0 = Analog loopback mode disabled. 1 = Enables external analog loopback mode.
2	Reserved	Read returns zero.
1	HBE	**Hybrid Enable.** 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable.** 0 = Receive path disabled. 1 = Enables receive path.

Register 3. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 4. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
Type		R	R	R/W	R/W	R	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	RDTN	**Ring Detect Signal Negative.** 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
4	OPOL	**Off-Hook Polarity.** 0 = Off-hook pin is active low. 1 = Off-hook pin is active high.
3	ONHM	**On-Hook Line Monitor.** 0 = Normal on-hook mode 1 = Enables low-power monitoring mode allowing the DSP to receive line activity without going off-hook. This mode is used for caller-ID detection. When the MODE bit is set to 1 (Register 18, bit 2), the device consumes ~7 µA from the phone line when in on-hook line monitor mode. When MODE = 0, the device consumes ~450 µA from the phone line when in on-hook line monitor mode. **Note:** This bit should be cleared before setting the OH bit. If using the $\overline{\text{OFHK}}$ pin to go off-hook, this bit should be cleared and one sample period should pass before driving the $\overline{\text{OFHK}}$ pin low.
2	RDT	**Ring Detect.** 0 = Reset either 4.5–9 seconds after last positive ring is detected or when the system executes an off-hook. 1 = Indicates a ring is occurring.
1	OHE	**Off-Hook Pin Enable.** 0 = Off-hook pin is ignored. 1 = Enables the operation of the off-hook pin.
0	OH	**Off-Hook.** 0 = Line-side device on-hook. 1 = Causes the line-side chip to go off-hook. This bit operates independently of the OHE bit and is a logic OR with the off-hook pin when enabled. When the MODE bit (Register 12, bit 2) is set to 1, the device will go on-hook without enabling the off-hook counter, thus allowing the device to go immediately (i.e., no timeout required on the counter) back off-hook when the MODE bit is cleared. This is useful in supporting Type II caller ID. **Note:** The ONHM bit should be cleared before setting this bit.

Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPE	ATM[1]	ARM[1]	PDL	PDN		ATM[0]	ARM[0]
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0111_0000

Bit	Name	Function
7	CPE	**Charge Pump Enable.** 0 = Charge pump is disabled. 1 = Charge pump is enabled. If the charge pump is not to be enabled, R3 must be installed with a 10 Ω, 1/10 W resistor and V_D must be between 4.75 and 5.25 V.
6,1	ATM[1:0]	**AOUT Transmit Path Level Control.** 00 = –20 dB transmit path attenuation for call progress AOUT pin only. 01 = –32 dB transmit path attenuation for call progress AOUT pin only. 10 = Mutes transmit path for call progress AOUT pin only. 11 = –26 dB transmit path attenuation for call progress AOUT pin only.
5,0	ARM[1:0]	**AOUT Receive Path Level Control.** 00 = 0 dB receive path attenuation for call progress AOUT pin only. 01 = –12 dB receive path attenuation for call progress AOUT pin only. 10 = Mutes receive path for call progress AOUT pin only. 11 = –6 dB receive path attenuation for call progress AOUT pin only.
4	PDL	**Power Down Line-Side Chip.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the Si3015 in lower power mode.
3	PDN	**Power Down.** 0 = Normal operation. 1 = Powers down the Si3021. A pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2	Reserved	Read returns zero.

Register 7. PLL1 Divide N1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1, 2)

Bit	Name	Function
7:0	N1[7:0]	**PLL N1 Divider.** Contains the (value – 1) for determining the output frequency on PLL1.

Register 8. PLL1 Divide M1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	M1							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1)

Reset settings = 0001_0011 (serial mode 2)

Bit	Name	Function
7:0	M1[7:0]	**PLL1 M1 Divider.** Contains the (value – 1) for determining the output frequency on PLL1.

Register 9. PLL2 Divide N2/M2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2				M2			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:4	N2[3:0]	**PLL2 N2 Divider.** Contains the (value – 1) for determining the output frequency on PLL2.
3:0	M2[3:0]	**PLL2 M2 Divider.** Contains the (value – 1) for determining the output frequency on PLL2.

Register 10. PLL Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								CGM
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	CGM	**Clock Generation Mode.** 0 = No additional ratio is applied to the PLL and faster lock times are possible. 1 = A 25/16 ratio is applied to the PLL allowing for a more flexible choice of MCLK frequencies while slowing down the PLL lock time.

Register 11. Chip A Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					REVA[3:0]			
Type					R			

Reset settings = N/A

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	REVA[3:0]	**Chip A Revision.** Four-bit value indicating the revision of the Si3021 (DSP-side) chip.

Register 12. Line Side Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLE	FDT			LCS[3:0]			
Type	R/W	R			R			

Reset settings = N/A

Bit	Name	Function
7	CLE	**Communications (ISOcap link) Error.** 0 = ISOcap communication link between Si3021 and Si3015 is operating correctly. 1 = Indicates a communication problem between the Si3021 and the Si3015. When it goes high, it remains high until a logic 0 is written to it.
6	FDT	**Frame Detect.** 0 = Indicates ISOcap link has not established frame lock. 1 = Indicates ISOcap link frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	LCS[3:0]	**Loop Current Sense.** Four-bit value returning the loop current for backward compatibility with the Si3034. It is decoded from the LVCS bits in Register 19. See LVCS bits for line voltage and current monitoring. When off-hook, these bits are decoded as follows from LVCS[4:0]: LCS[3:0] = LVCS[4:1] except when LVCS[4:0] = 11110, LCS[3:0] = 1110 or when LVCS[4:0] = 00001, LCS[3:0] = 0001 When on-hook, LCS[3:0] = LVCS[4:1].

Register 13. Chip B Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CBID	REVB[3:0]				ARXB	ATXB
Type	R		R				R/W	R/W

Reset settings = N/A

Bit	Name	Function
7	Reserved	Read returns zero.
6	CBID	**Chip B ID.** 0 = Indicates the line side is domestic only. 1 = Indicates the line side has international support.
5:2	REVB[3:0]	**Chip B Revision.** Four-bit value indicating the revision of the Si3015 (line side) chip.
1	ARXB	**Receive Gain.** 0 = 0 dB gain is applied. 1 = A 6 dB gain is applied to the receive path. **Note:** This bit is for Si3032 backwards compatibility. The Si3044 has additional receive gain settings ARX[2:0] in Register 15. ARXB should be set to 0 if the settings in Register 15 are used.
0	ATXB	**Transmit Attenuation.** 0 = 0 dB gain is applied. 1 = A 3 dB attenuation is applied to the transmit path. **Note:** This bit is for Si3032 backwards compatibility. The Si3044 has additional transmit gain settings ATX[2:0] in Register 15. ATXB should be set to 0 if the settings in Register 15 are used.

Register 14. Daisy Chain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
Type	R/W			R/W		R/W	R/W	R/W

Reset settings = 0000_0010 (serial mode 0,1)

Reset settings = 0011_1111 (serial mode 2)

Bit	Name	Function
7:5	NSLV[2:0]	**Number of Slaves devices.** 000 = 0 slaves. Simply redefines the FC/$\overline{\text{RGDT}}$ and $\overline{\text{RGDT}}$/FSD pins. 001 = 1 slave device 010 = 2 slave devices 011 = 3 slave devices 100 = 4 slave devices (For four or more slave devices, the FSD bit MUST be set.) 101 = 5 slave devices 110 = 6 slave devices 111 = 7 slave devices
4:3	SSEL[1:0]	**Slave device select.** 00 = 16-bit SDO receive data 01 = Reserved 10 = 15-bit SDO receive data. LSB = 1 for the Si3044 device. 11 = 15-bit SDO receive data. LSB = 0 for the Si3044 device.
2	FSD	**Delayed Frame Sync Control.** 0 = Sets the number of SCLK periods between frame syncs to 32. 1 = Sets the number of SCLK periods between frame syncs to 16. This bit **MUST** be set when Si3044 devices are slaves. For the master Si3044, only serial mode 1 is allowed in this case.
1	RPOL	**Ring Detect Polarity.** 0 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active low. 1 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active high.
0	DCE	**Daisy-Chain Enable.** 0 = Daisy-chaining disabled. 1 = Enables the Si3044 to operate with slave devices on the same serial bus. The FC/$\overline{\text{RGDT}}$ signal (pin 7) becomes the ring detect output and the $\overline{\text{RDGT}}$/FSD signal (pin 15) becomes the delayed frame sync signal. Note that **ALL** other bits in this register are ignored if DCE = 0.

Register 15. TX/RX Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX[2:0]			RXM	ARX[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute.** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation 001 = 3 dB attenuation 010 = 6 dB attenuation 011 = 9 dB attenuation 1xx = 12 dB attenuation **Note:** Register 13 ATXB bit must be 0 if these bits are used.
3	RXM	**Receive Mute.** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain/On-Hook Line Monitor Receive Attenuation.** This register functions as both a gain setting for the regular DAA receive path and an attenuation setting for the new low-power on-hook line monitor ADC receive path. **Receive Gain** — **On-Hook Line Monitor Attenuation** 000 = 0 dB gain — 000 = 0 dB attenuation 001 = 3 dB gain — 001 = 1 dB attenuation 010 = 6 dB gain — 010 = 2.2 dB attenuation 011 = 9 dB gain — 011 = 3.5 dB attenuation 1xx = 12 dB gain — 1xx = 5 dB attenuation **Note:** Register 13 ARXB bit must be 0 if these bits are used.

Register 16. International Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OFF/SQL2	OHS	ACT	IIRE	DCT[1:0]		RZ	RT
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0000_1000

Bit	Name	Function
7	OFF/SQL2	**DC Termination Off (DAA is off-hook).** When the DAA is off-hook, this bit functions as the DC Termination Off bit. For Si3015 line-side devices revision D and later, when the DAA is on-hook, this bit functions as the Enhanced Ring Detect Network Squelch bit. For Si3015 line-side devices revision C and earlier, this bit only functions as the DC Termination Off bit. 0 = Normal operation 1 = DC termination disabled and the device presents an 800 Ω DC impedance to the line which is used to enhance operation with a parallel phone. The DCT pin voltage is also reduced for improved low line voltage performance. **Enhanced Ring Detect Network Squelch (DAA is on-hook. Valid only for Si3015 line-side devices revision D and later).** To properly receive caller ID data, this bit must be set following a polarity reversal or ring signal detection and must be left enabled during the reception of caller ID data. It should be disabled before the start of the next ring signal. It is used to recover the offset on the RNG1/2 pins after a polarity reversal or ring signal. 0 = Normal operation. 1 = Enhanced squelch function is enabled.
6	OHS	**On-Hook Speed.** 0 = The Si3044 will execute a fast on-hook. (Off-hook counter = 1024/Fs seconds.) 1 = The Si3044 will execute a slow, controlled on-hook. (Off-hook counter = 4096/Fs seconds.)
5	ACT	**AC Termination Select.** 0 = Selects the real impedance. 1 = Selects the complex impedance.
4	IIRE	**IIR Filter Enable.** 0 = FIR filter enabled for transmit and receive filters. (See Figures 6–9 on page 13.) 1 = IIR filter enabled for transmit and receive filters. (See Figures 10–15 on page 14.)
3:2	DCT[1:0]	**DC Termination Select.** 00 = Low Voltage Mode. (Transmit level = –5 dBm) 01 = Japan Mode. Lower voltage mode. (Transmit level = –3 dBm) 10 = FCC Mode. Standard voltage mode. (Transmit level = –1 dBm) 11 = CTR21 Mode. Current limiting mode. (Transmit level = –1 dBm)

Bit	Name	Function
1	RZ	**Ringer Impedance.** 0 = Maximum (high) ringer impedance. 1 = Synthesize ringer impedance. C15, R14, Z2, and Z3 must not be installed when setting this bit. See "Ringer Impedance" on page 25.
0	RT	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level will not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. 0 = 11 to 22 Vrms 1 = 17 to 33 Vrms

Register 17. International Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MCAL	CALD	LIM	OPE	BTE	ROV	BTD
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Must be zero.
6	MCAL	**Manual Calibration.** 0 = No calibration. 1 = Initiate calibration.
5	CALD	**Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
4	LIM	**Current Limit** 0 = All other modes. 1 = CTR21 mode with current limiting enabled.
3	OPE	**Overload Protect Enable.** 0 = Disable overload protection. 1 = Enable overload protection. The overload protection feature prevents damage to the DAA when going off-hook with excessive line current or voltage. When off-hook, if OPE is set and LVCS = 11111, the DC termination is disabled (800 Ω presented to the line), the hookswitch current is reduced, and the OPD bit (Register 19) is set. The OPE bit should be written ~25 ms after going off-hook; it should be written to 0 to reset.

Bit	Name	Function
2	BTE	**Billing Tone Protect Enable.** 0 = Billing tone protection disabled. 1 = Billing tone protection enabled. When set, the Si3044 will automatically respond to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 and BTD goes high, the DC termination is changed to present 800 Ω to the line, and the DCT pin stops tracking the receive input pin. During normal operation, the DCT pin tracks the receive input. **Note:** On the Si3044, the BTD and ROV bits are always enabled (after the delayed off-hook counter). On the Si3034, these bits were enabled only when BTE = 1.
1	ROV	**Receive Overload.** This bit is set when the receive input has an excessive input level (i.e., receive pin goes below ground). This bit is cleared by writing a zero to this location. 0 = Normal receive input level. 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** This bit will be set if a billing tone is detected. This bit is cleared by writing a zero to this location. 0 = No billing tone detected. 1 = Billing tone detected.

Register 18. International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FULL	DIAL	FJM	VOL	FLVM	MODE	RFWE	SQLH
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	FULL	**Full Scale.** 0 = Default. 1 = Transmit/receive full scale = +3.2 dBm. This bit changes the full scale of the ADC and DAC from –1 dBm min to +3.2 dBm min. When this bit is set, R2 must be changed from 402 Ω to 243 Ω. This mode, which can be useful for certain voice applications, should only be used in the FCC/600 Ω AC Termination mode.
6	DIAL	**DTMF Dialing Mode.** This bit should be set during DTMF dialing in CTR21 mode if LCS[3:0] < 6 or LVCS[4:0] < 12 decimal. 0 = Normal operation. 1 = Increase headroom for DTMF dialing.
5	FJM	**Force Japan DC Termination Mode.** 0 = Normal Gain. 1 = When Register 16, DCT[1:0], is set to 10b (FCC mode), setting this bit will force the Japan DC termination mode while allowing for a transmit level of –1 dBm. See "DTMF Dialing" on page 26.
4	VOL	**Line Voltage Adjust.** When set, this bit will adjust the TIP-RING line voltage. Lowering this voltage will improve margin in low voltage countries. Raising this voltage may improve large signal distortion performance. 0 = Normal operation. 1 = Lower DCT voltage.

Description	DCT	OFF	VOL	VDCT	DELTA
CTR21/FCC	1x	0	0	4.00	
CTR21/FCC+VOL	1x	0	1	3.51	0.49 V
JAPAN	01	0	0	3.15	
JAPAN+VOL	01	0	1	2.87	0.28 V
LVMode	00	0	0	2.65	
LVMode+VOL	00	0	1	2.47	0.18 V
CTR21/FCC+OFF	1x	1	0	2.33	
CTR21/FCC+VOL+OFF	1x	1	1	2.21	0.12 V
JAPAN+OFF	01	1	0	2.10	
JAPAN+VOL+OFF	01	1	1	2.01	0.09 V
LVMode+OFF	00	1	0	1.94	
LVMode+VOL+OFF	00	1	1	1.87	0.07 V

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>3</td><td>FLVM</td><td>Force Low Voltage DC Termination Mode.
0 = Normal gain.
1 = When Register 16, DCT[1:0], is set to 10b (FCC mode), setting this bit will force the Low Voltage DC termination mode while allowing for a transmit level of –1 dBm. See "DTMF Dialing" on page 26.</td></tr>
<tr><td>2</td><td>MODE</td><td>MODE Control.
This bit is used to enable the on-hook line monitor ADC and the line voltage monitor.
<table>
<tr><th>MODE</th><th>OH</th><th>ONHM</th><th>Line Function</th><th>SDO</th><th>LVCS[4:0]</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>on-hook</td><td>ring data</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>on-hook</td><td>line data using the higher current line monitor</td><td>11111 if a line voltage exists, or 00000 if no line voltage exists</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>off-hook</td><td>line data</td><td>loop current</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>off-hook/Fast DCT mode</td><td>line data</td><td>loop current</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>on-hook</td><td>ring data</td><td>line voltage</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>on-hook</td><td>line data using the low current line monitor</td><td>line voltage</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>force on-hook</td><td>no data is transmitted on SDO in this mode</td><td>line voltage</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>force on-hook</td><td>line data using the low current line monitor</td><td>line voltage</td></tr>
</table>
Notes:
1. If RZ = 1, LVCS[4:0] = either 11111 or 00000 during a ring event. All ones are shown if a line voltage exists; all zeroes are shown if no line voltage exists.
2. Force on-hook mode puts the Si3015 into an on-hook state without restarting the off-hook counter. This is used to support Type II caller ID.
3. The MODE bit is in a different register (Register 18) than the OH and ONHM bits (Register 5). The user should write the registers in a sequence so as not to pass through an undesired state.
4. Fast DCT mode puts the Si3015 into an off-hook state that is intended to quickly settle the line voltage just after going off-hook. While in this mode, data transmission is not recommended. This is used to support Type II caller ID.
5. The ONHM bit should be cleared before setting the OH bit. If both bits need to be set, the OH bit should be set first, and then the ONHM bit should be set in a separate register access.</td></tr>
<tr><td>1</td><td>RFWE</td><td>Ring Detector Full Wave Rectifier Enable.
When set, the ring detection circuitry provides full-wave rectification. This will affect the $\overline{\text{RGDT}}$ pin as well as the data stream presented on SDO during ring detection.
0 = Half Wave.
1 = Full Wave.</td></tr>
<tr><td>0</td><td>SQLH</td><td>Ring Detect Network Squelch.
This bit must be set, then cleared after at least 1 ms, following a polarity reversal or ring signal detection. It is used to quickly recover the offset on the RNG1/2 pins after a polarity reversal or ring signal.
0 = Normal operation.
1 = Squelch function is enabled.</td></tr>
</table>

Register 19. International Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LVCS					OVL	DOD	OPD
Type	R					R	R	R

Reset settings = 0000_0000

Bit	Name	Function
7:3	LVCS[4:0]	**Line Voltage/Current Sense.** Represents either the line voltage, loop current, or on-hook line monitor depending on the state of the MODE, OH, and ONHM bits. **On-Hook Voltage Monitor (2.75 V/bit)** 00000 = No line connected. 00001 = Minimum line voltage (V_{MIN} = 3 V ± 0.5 V). 11111 = Maximum line voltage (87 V ± 20%). The line voltage monitor full scale may be modified by changing R5 as follows: $V_{MAX} = V_{MIN} + 4.2\ (10M + R5 + 1.6k)/[(R5 + 1.6k)*5]$ **Off-Hook Loop Current Monitor (3 mA/bit)** 00000 = Loop current is less than required for normal operation. 00001 = Minimum normal loop current. 11110 = Maximum normal loop current. 11111 = Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21 Overload > 54 mA in CTR21 mode
2	OVL	**Overload Detected.** This bit has the same function as ROV in Register 17, but will clear itself after the overload has been removed. See “Billing Tone Detection” on page 26. This bit is only masked by the off-hook counter and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
1	DOD	**Recal/Dropout Detect.** When the line-side device is off-hook, it is powered from the line itself. If this line-derived power supply collapses, such as when the line is disconnected, this bit is set to 1. Sixteen frames (16/Fs) after the line-derived power supply returns, this bit is set to 0. When on-hook, this bit is set to 0. 0 = Normal operation. 1 = Line supply dropout detected when on-hook.
0	OPD	**Overload Protect Detected.** 0 = Inactive. 1 = Overload protection active. **Note:** See description of overload protect operation (OPE bit, Register 17).

APPENDIX—UL1950 3RD EDITION

Although designs using the Si3044 comply with UL1950 3rd Edition and pass all over-current and over-voltage tests, there are still several issues to consider.

Figure 39 shows two designs that can pass the UL1950 overvoltage tests, as well as electromagnetic emissions. The top schematic of Figure 39 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 39 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests will apply to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your professional testing agency during the design of the product to determine which tests apply to your system.

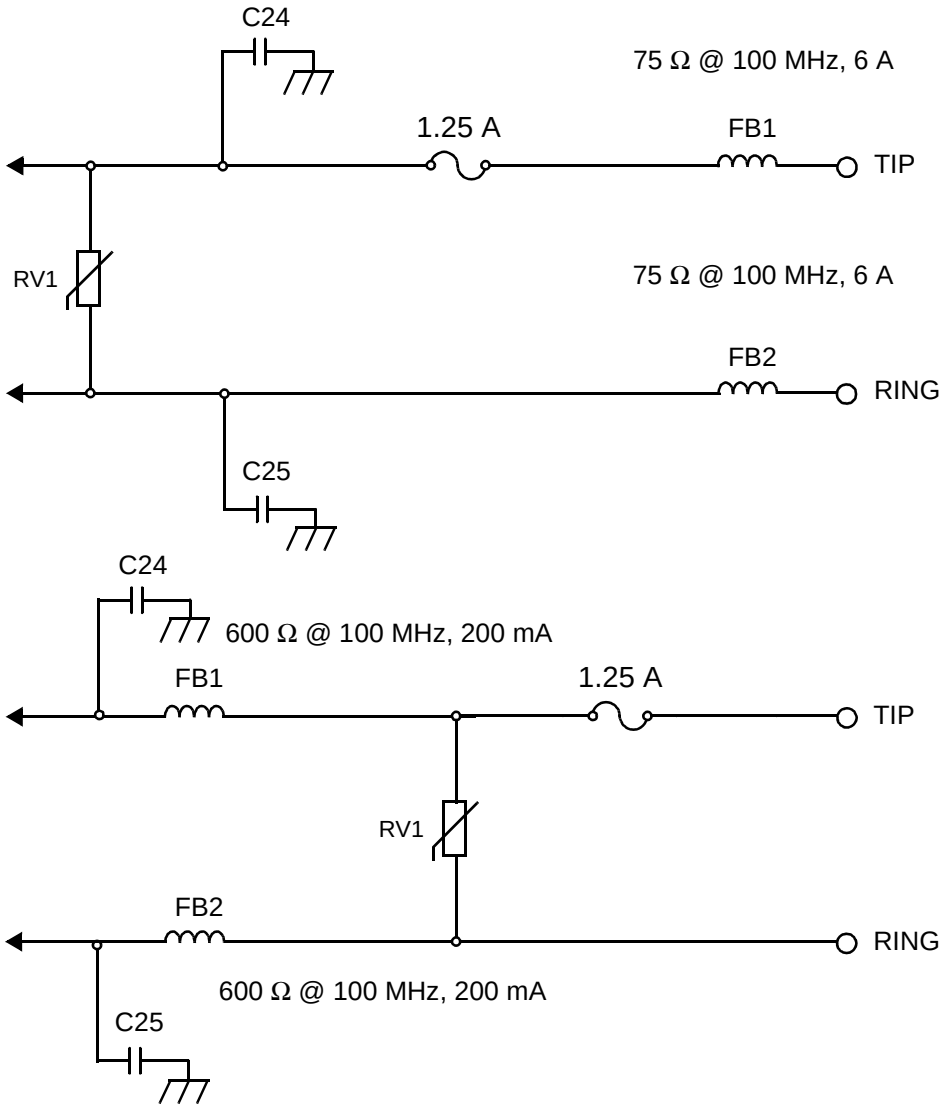


Figure 39. Circuits that Pass all UL1950 Overvoltage Tests

Pin Descriptions: Si3021

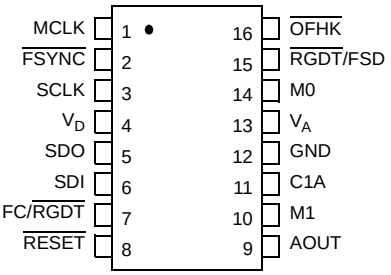


Table 26. Si3021 Pin Descriptions

Pin #	Pin Name	Description
1	MCLK	**Master Clock Input.** High speed master clock input. Generally supplied by the system crystal clock or modem/DSP.
2	$\overline{\text{FSYNC}}$	**Frame Sync Output.** Data framing signal that is used to indicate the start and stop of a communication/data frame.
3	SCLK	**Serial Port Bit Clock Output.** Controls the serial data on SDO and latches the data on SDI.
4	V_D	**Digital Supply Voltage.** Provides the digital supply voltage to the Si3021, nominally either 5 V or 3.3 V.
5	SDO	**Serial Port Data Out.** Serial communication data that is provided by the Si3021 to the modem/DSP.
6	SDI	**Serial Port Data In.** Serial communication and control data that is generated by the modem/DSP and presented as an input to the Si3021.
7	FC/$\overline{\text{RGDT}}$	**Secondary Transfer Request Input/Ring Detect.** An optional signal to instruct the Si3021 that control data is being requested in a secondary frame. When daisy chain is enabled, this pin becomes the ring detect output. Produces an active low rectified version of the ring signal.
8	$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined, initialized state. Also used to bring the Si3044 out of sleep mode.
9	AOUT	**Analog Speaker Out.** Provides an analog output signal for driving a call progress speaker.
10	M1	**Mode Select 1.** The second of two mode select pins that is used to select the operation of the serial port/DSP interface.

Table 26. Si3021 Pin Descriptions (Continued)

Pin #	Pin Name	Description
11	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor C1. Used to communicated with the line-side device.
12	GND	**Ground.** Connects to the system digital ground.
13	V_A	**Analog Supply Voltage.** Provides the analog supply voltage for the Si3021, nominally 5 V. This supply is typically generated internally with an on-chip charge pump set through a control register.
14	M0	**Mode Select 0.** The first of two mode select pins that is used to select the operation of the serial port/ DSP interface.
15	$\overline{\text{RGDT}}$/FSD	**Ring Detect/Delayed Frame Sync.** Output signal that indicates the status of a ring signal. Produces an active low rectified version of the ring signal. When daisy chain is enabled, this signal becomes a delayed frame sync to drive a slave device.
16	$\overline{\text{OFHK}}$	**Off-Hook.** An active low input control signal that provides a termination across TIP and RING for line seizing and pulse dialing.

Pin Descriptions: Si3015

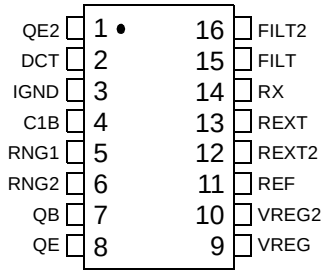


Table 27. Si3015 Pin Descriptions

Pin #	Pin Name	Description
1	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
2	DCT	**DC Termination.** Provides DC termination to the telephone network.
3	IGND	**Isolated Ground.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side device.
5	RNG1	**Ring 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3044.
6	RNG2	**Ring 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3044.
7	QB	**Transistor Base.** Connects to the base of transistor Q3. Used to go on/off-hook.
8	QE	**Transistor Emitter.** Connects to the emitter of transistor Q3. Used to go on/off-hook.
9	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**Reference.** Connects to an external resistor to provide a high accuracy reference current.
12	REXT2	**External Resistor 2.** Sets the complex AC termination impedance.

Table 27. Si3015 Pin Descriptions (Continued)

Pin #	Pin Name	Description
13	REXT	**External Resistor.** Sets the real AC termination impedance.
14	$\overline{\text{RX}}$	**Receive Input.** Serves as the receive side input from the telephone network.
15	FILT	**Filter.** Provides filtering for the DC termination circuits.
16	FILT2	**Filter 2.** Provides filtering for the bias circuits.

Ordering Guide

Table 28. Ordering Guide

Chipset	Region	Interface	Digital	Line	Temperature
Si3034	Global	DSP Serial I/F	Si3021-KS	Si3014-KS	0°C to 70°C
Si3035	FCC/Japan	DSP Serial I/F	Si3021-KS	Si3012-KS	0°C to 70°C
Si3036	FCC/Japan	AC Link	Si3024-KS	Si3012-KS	0°C to 70°C
Si3038	Global	AC Link	Si3024-KS	Si3014-KS	0°C to 70°C
Si3044	Enhanced Global	DSP Serial I/F	Si3021-KS	Si3015-KS	0°C to 70°C
Si3044	Enhanced Global	DSP Serial I/F	Si3021-BS	Si3015-BS	–40°C to 85°C

Package Outline

Figure 40 illustrates the package details for the Si3021 and Si3015. Table 29 lists the values for the dimensions shown in the illustration.

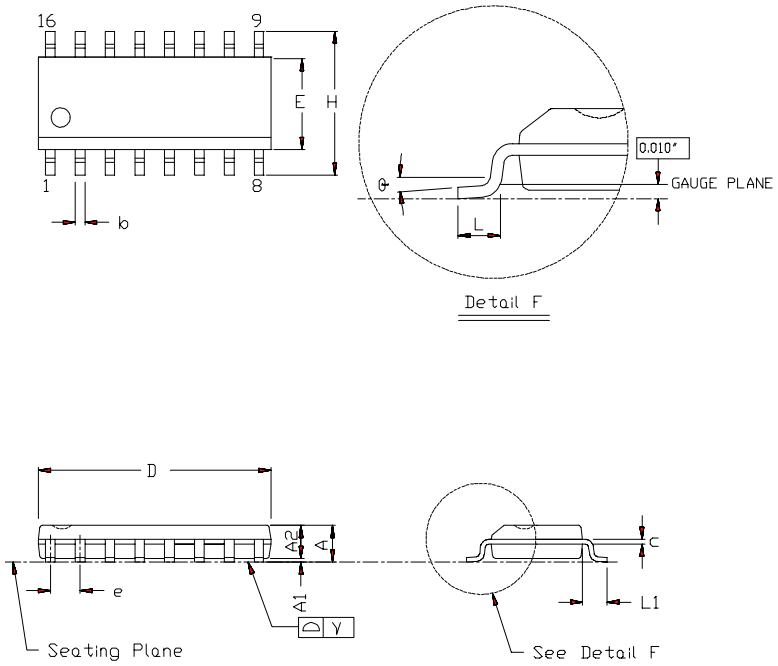


Figure 40. 16-pin Small Outline Plastic Package (SOIC)

Table 29. Package Diagram Dimensions

Controlling Dimension: mm

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.051	0.059	1.30	1.50
b	0.013	0.020	0.330	0.51
c	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC	—	1.27 BSC	—
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
L1	0.042 BSC	—	1.07 BSC	—
γ	—	0.004	—	0.10
θ	0°	8°	0°	8°

Rev 0.4 to Rev 0.5 Change List

- Typical Application Circuit updated.
- C24, C25 value changed from 470 pF to 1000 pF and C31, C32 were added in Table 13 and Table 14. In Table 14, the tolerance was also changed from 20% to 10%.
- In Table 17, the Register 17 heading changed from LIM[1:0] to LIM, and the numbers in the column below were reduced from two digits to one.

Rev 0.5 to Rev 1.0 Change List

- 20 μA on-hook line monitor current changed to 7 μA.
- Table 2 updated.
- Table 5 updated.
- Table 7 updated.
- Global component values for Q4 updated.
- “Upgrading from Si3034 to Si3044” updated.
- “On-Chip Charge Pump” section added.
- “DC Termination” updated.
- “DTMF Dialing” updated.
- “Billing Tone Detection” updated.
- “On-Hook Line Monitor” updated.
- “Multiple Device Support” updated.
- “Revision Identification” updated.
- Register 15 updated.
- Register 16 updated.
- FLVM bit added to Register 18.
- Register 19 updated.

Rev 1.0 to Rev 1.1 Change List.

- Table 2 updated (note added).
- Table 5 updated (note added)
- Textual additions were made concerning the necessity of disabling the on-hook line monitor feature before putting the device into an off-hook state.

NOTES:

NOTES:

Contact Information

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com