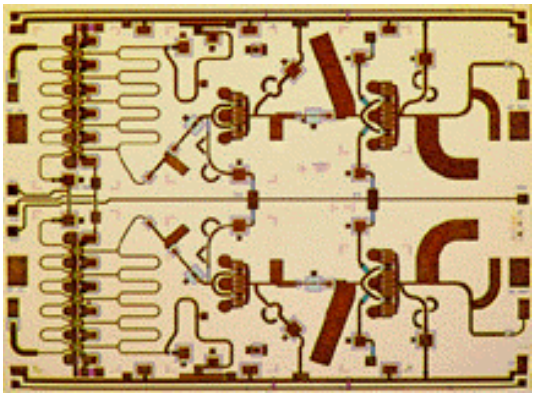
TriQuint SEMICONDUCTOR

Product Data Sheet

June 5, 2001

6 - 17 GHz Dual-Channel Power Amplifier TGA6316-EEU



Key Features and Performance

- 6 to 17 GHz Frequency Range
- Dual Channel Power Amplifier
- 20.5dB Typical Gain, Single Channel
- 1.5:1 Typical Input SWR, 2.1:1 Typical Output SWR, Single Channel
- 29.5 dBm Output Power at 3 dB Gain Compression, (31dBm combined)
- 6.5024 x 4.8006 x 0.1016 mm (0.256 x 0.189 x 0.004 in.)

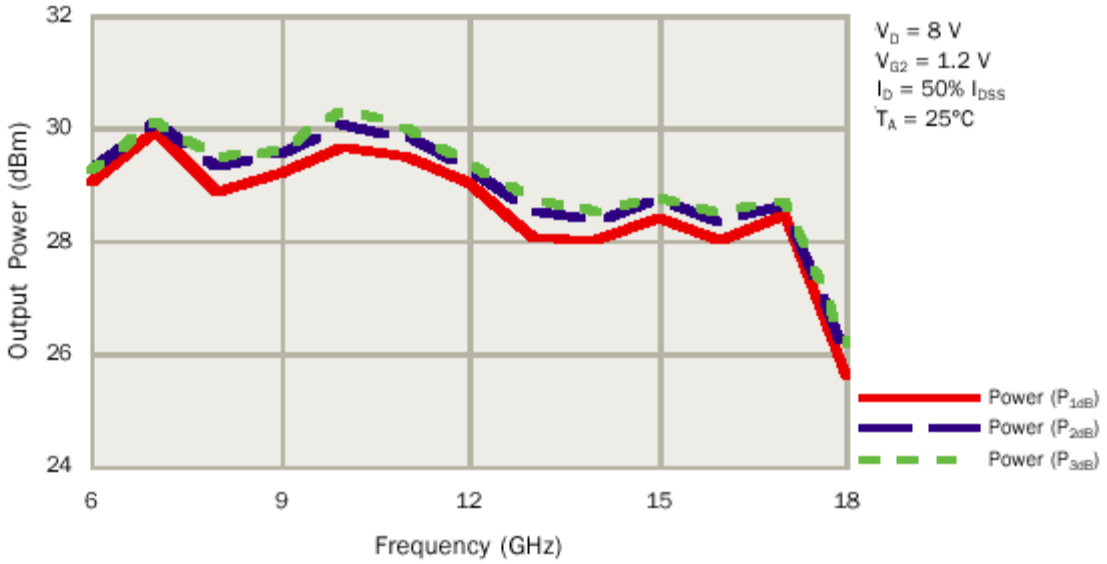
Description

The TriQuint TGA6316-EEU is a dual channel GaAs monolithic amplifier which operates from 6 to 17-GHz. Each channel features three-stage topology with a 1200-mm dual-gate FET distributed amplifier for the first stage, a 1200 µm single gate FET second stage, and a 1900 µm single gate FET third stage. The dual-channel construction is designed for off-chip combining.

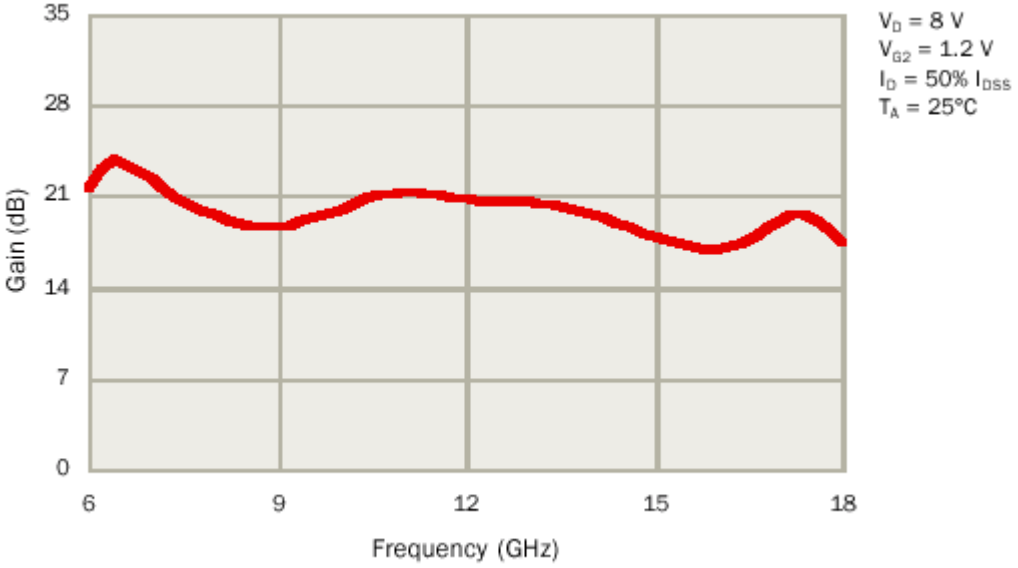
A single channel of the TGA6316-EEU provides 20.5-dB typical small signal gain and 29.5 dBm output power at 3 dB gain compression. The TGA6316-EEU amplifier is designed for use in wideband systems such as electronic warfare, expendable decoys and test equipment.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. Ground is provided to the circuitry through vias to the backside metallization.

TYPICAL OUTPUT POWER FOR SINGLE CHANNEL



TYPICAL SMALL-SIGNAL POWER GAIN FOR SINGLE CHANNEL



TYPICAL RETURN LOSS FOR SINGLE CHANNEL

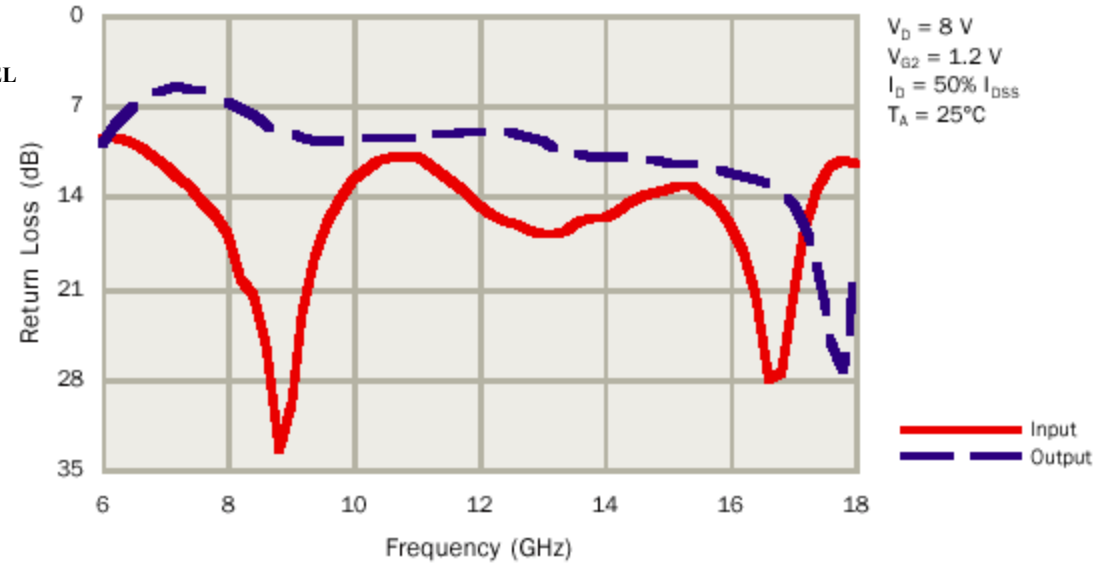


TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V_D	POSITIVE SUPPLY VOLTAGE	9V
$V_D - V_{G1}$	POSITIVE SUPPLY VOLTAGE RANGE WITH RESPECT TO NEGATIVE SUPPLY VOLTAGE	0V to 10V
V_{G1}	NEGATIVE SUPPLY VOLTAGE RANGE	-5V to 0V
V_{G2}	GAIN CONTROL VOLTAGE RANGE	-5V to 4V
$V_{G2} - V_D$	GAIN CONTROL VOLTAGE RANGE WITH RESPECT TO POSITIVE SUPPLY VOLTAGE	0V to –10V
I_D	POSITIVE SUPPLY CURRENT	I_{DSS}
I^-	NEGATIVE SUPPLY CURRENT	-9.7mA
P_D	POWER DISSIPATION, AT (OR BELOW) 25°C BASE-PLATE TEMPERATURE *	25dBm
T_{CH} **	OPERATING CHANNEL TEMPERATURE	150 ^{0}C
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 ^{0}C
T_{STG}	STORAGE TEMPERATURE	-65 to 150 ^{0}C

Ratings over channel operating temperature range, T_{CH} (unless otherwise noted)

Stresses beyond those listed under “Maximum Ratings” may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “RF Specifications” is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

*For operation above 25°C base-plate temperature, derate linearly at the rate of 21.7mW/°C.
** Operating channel temperature, T_{CH}, directly affects the device MTTF. For maximum life, it is recommended that channel temperature be maintained at the lowest possible level.

TABLE II
DC PROBE TESTS (100%)

NOTES	SYMBOL	TEST CONDITIONS (T_A = 25 °C ± 5 °C)	LIMITS		UNITS
			MIN	MAX	
2/	I_{DSS1}	STD except gate2 is set to 1.0V	271	514	mA
2/	I_{DSS2}	STD	271	514	mA
2/	I_{DSS3}	STD	429	814	mA
2/	I_{DSS4}	STD except gate2 is set to 1.0V	271	514	mA
2/	I_{DSS5}	STD	271	514	mA
2/	I_{DSS6}	STD	429	814	mA
2/	G_{m1}	STD except gate2 is set to 1.0V	108	228	mS
2/	G_{m2}	STD	108	228	mS
2/	G_{m3}	STD	171	361	mS
2/	G_{m4}	STD except gate2 is set to 1.0V	108	228	mS
2/	G_{m5}	STD	108	228	mS
2/	G_{m6}	STD	171	361	mS
1/,2/	$\|V_{P1G1}\|$	STD	2	4.6	V
1/,2/	$\|V_{P1G2}\|$	STD	2	4.6	V
1/,2/	$\|V_{P2}\|$	STD	2	4.6	V
1/,2/	$\|V_{P3}\|$	STD	2	4.6	V
1/,2/	$\|V_{P4G1}\|$	STD	2	4.6	V
1/,2/	$\|V_{P4G2}\|$	STD	2	4.6	V
1/,2/	$\|V_{P5}\|$	STD	2	4.6	V
1/,2/	$\|V_{P6}\|$	STD	2	4.6	V
1/,2/	$\|V_{BRGD2,3}\|$	-4.6 delta applied to gate1, gate2	6	30	V
1/,2/	$\|V_{BRGD5,6}\|$	-4.6 delta applied to gate1, gate2	6	30	V
1/,2/	$\|V_{BRGS1}\|$	STD	6	30	V
1/,2/	$\|V_{BRGS2}\|$	STD	6	30	V
1/,2/	$\|V_{BRGS3}\|$	STD	6	30	V
1/,2/	$\|V_{BRGS4}\|$	STD	6	30	V
1/,2/	$\|V_{BRGS5}\|$	STD	6	30	V
1/,2/	$\|V_{BRGS6}\|$	STD	6	30	V

1/ V_P, V_{BRGD}, and V_{BRGS} are negative.

2/ STD refers to Standard Test Conditions, see Table IV

TABLE III

RF SPECIFICATIONS

(T_A = 25°C ± 5°C)

V^+ = 8V, I^+ = 704mA, V_{G2} = 1.2V (single channel)

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL-SIGNAL GAIN MAGNITUDE	F = 6 – 17 GHz	14	20.5	25	dB
	POWER OUTPUT AT 3dB COMPRESSION	F = 6 – 17 GHz		29.5		dB
	POWER OUTPUT AT 2dB COMPRESSION	F = 6 – 17 GHz	27.5	29		dB
	POWER OUTPUT AT 1dB GAIN COMPRESSION	F = 6 – 17 GHz	25	28.5		dBm
	INPUT RETURN LOSS MAGNITUDE	F = 6 – 17 GHz	7.4			dB
	OUTPUT RETURN LOSS MAGNITUDE	F = 6 – 9 GHz F = 9 – 17 GHz	4 6.5			dB dB
	INPUT STANDING WAVE RATIO	F = 6 – 17 GHz		1.5:1		
	OUTPUT STANDING WAVE RATIO	F = 6 – 17 GHz		2.1:1		

TABLE IV
AUTOPROBE FET PARAMETER MEASUREMENT CONDITONS

FET Parameters	Test Conditions
I_{DSS} : Maximum drain current (I_{DS}) with gate voltage (V_{GS}) at zero volts.	V_{GS} = 0.0 V, drain voltage (V_{DS}) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of I_{DS}; voltage for I_{DSS} is recorded as VDSP.
G_m : Transconductance; $\frac{(I_{DSS} - IDS1)}{VG1}$	For all material types, V_{DS} is swept between 0.5 V and VDSP in search of the maximum value of I_{ds}. This maximum I_{DS} is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at V_{GS} = VG1 = -0.5 V. For Low Noise, HFET and pHEMT material, V_{GS} = VG1 = -0.25 V. For LNBECOLC, use V_{GS} = VG1 = -0.10 V.
V_P : Pinch-Off Voltage; V_{GS} for I_{DS} = 0.5 mA/mm of gate width.	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I_{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V_{GD}) measured is V_{BVGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I_{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V_{GS}) measured is V_{BVGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

TYPICAL S-PARAMETERS

Frequency	S_{11}		S_{21}		S_{12}		S_{22}		GAIN
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	(dB)
6.0	0.34	-162	11.98	25	0.004	13	0.32	-13	21.6
6.4	0.33	179	15.41	-60	0.001	146	0.43	-57	23.8
6.8	0.29	162	13.82	-131	0.001	136	0.50	-92	22.8
7.2	0.24	150	12.11	170	0.001	127	0.53	-122	21.7
7.6	0.19	138	10.41	122	0.001	126	0.51	-147	20.3
8.0	0.14	126	9.49	77	0.001	135	0.47	-171	19.5
8.4	0.08	117	8.74	37	0.001	136	0.41	171	18.8
8.8	0.02	143	8.54	-2	0.001	126	0.36	156	18.6
9.2	0.07	-126	8.64	-38	0.001	139	0.33	143	18.7
9.6	0.16	-140	9.24	-77	0.001	119	0.33	130	19.3
10.0	0.23	-161	9.89	-116	0.002	124	0.33	114	19.9
10.4	0.28	178	10.93	-158	0.002	81	0.34	97	20.8
10.8	0.29	157	11.42	158	0.002	85	0.34	79	21.2
11.2	0.27	136	11.58	114	0.000	30	0.35	61	21.3
11.6	0.23	122	11.23	71	0.001	23	0.35	41	21.0
12.0	0.19	112	11.05	29	0.001	-75	0.36	21	20.9
12.4	0.16	110	10.76	-12	0.001	-142	0.35	1	20.6
12.8	0.15	108	10.82	-54	0.001	-147	0.34	-20	20.7
13.2	0.14	107	10.48	-97	0.000	124	0.31	-37	20.4
13.6	0.16	107	10.21	-141	0.002	147	0.29	-51	20.2
14.0	0.16	99	9.47	177	0.001	157	0.28	-63	19.5
14.4	0.19	94	8.89	133	0.000	-121	0.28	-78	19.0
14.8	0.21	81	8.09	92	0.001	171	0.27	-91	18.2
15.2	0.22	63	7.56	51	0.000	-105	0.27	-104	17.6
15.6	0.20	43	7.09	11	0.001	-120	0.26	-118	17.0
16.0	0.16	24	7.06	-28	0.002	-142	0.25	-131	17.0
16.4	0.08	13	7.41	-69	0.001	-142	0.24	-144	17.4
16.8	0.04	97	8.52	-115	0.001	-115	0.21	-160	18.6
17.2	0.15	109	9.45	-174	0.001	-174	0.15	-177	19.5
17.6	0.26	78	9.15	121	0.000	-30	0.06	-179	19.2
18.0	0.27	43	7.29	58	0.000	-57	0.11	-84	17.3

T_A = 25°C, V_D = 8 V, V_{G2} = 1.2 V, I_D = 50% I_{DSS} (single channel)

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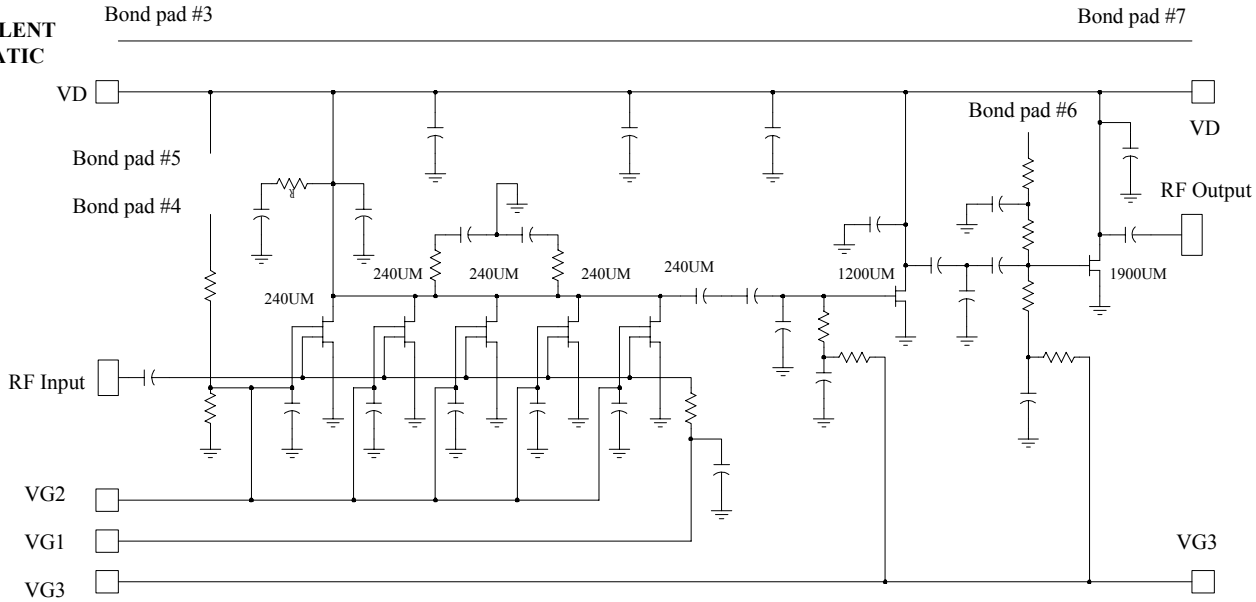
EQUIVALENT SCHEMATIC

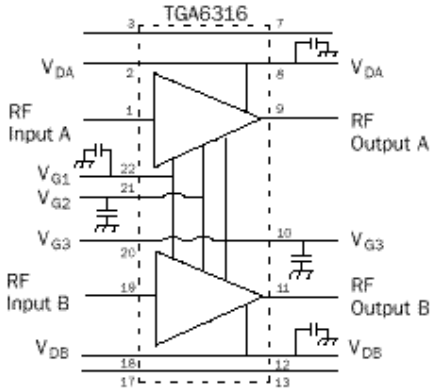


Bond pad #3 and Bond pad #7 are extra transmission lines that can be used for bias routing through a module.

This device offers an optional gate 2 bias for the first stage. Instead of using the VG2 pad, bond a wire from Bond pad #4 to Bond pad #5 to apply 1.5 V to gate 2 of the first stage with VD = 8V.

Bond pad #6 is not used.

RECOMMENDED BIAS NETWORK



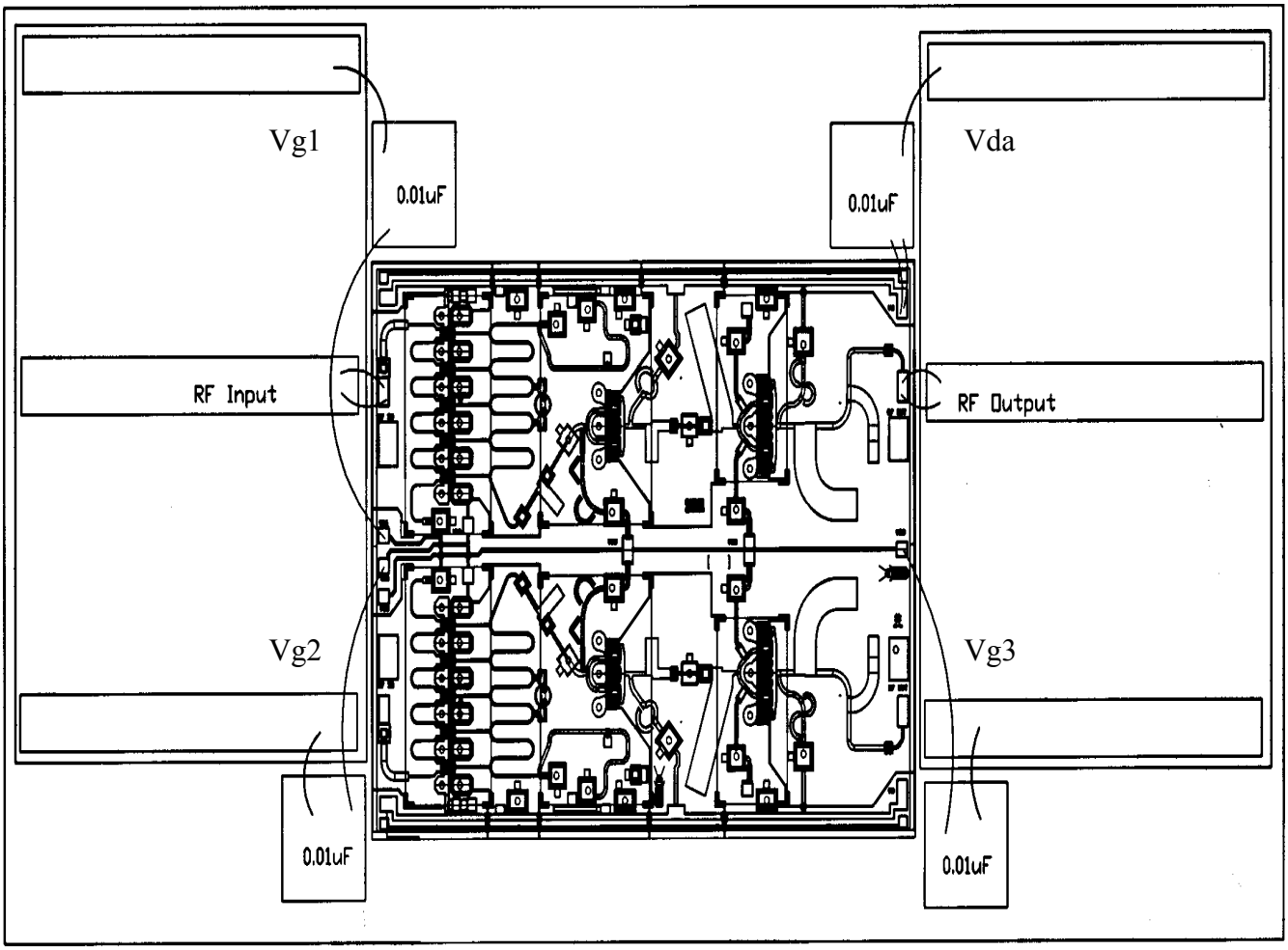
RF connections: Bond using two 1-mil-diameter, 20 to 25-mil-length gold bond wires at both RF Input and RF Output for optimum RF performance.

The capacitors used were 0.01 uF.

Close placement of external components is essential to stability.

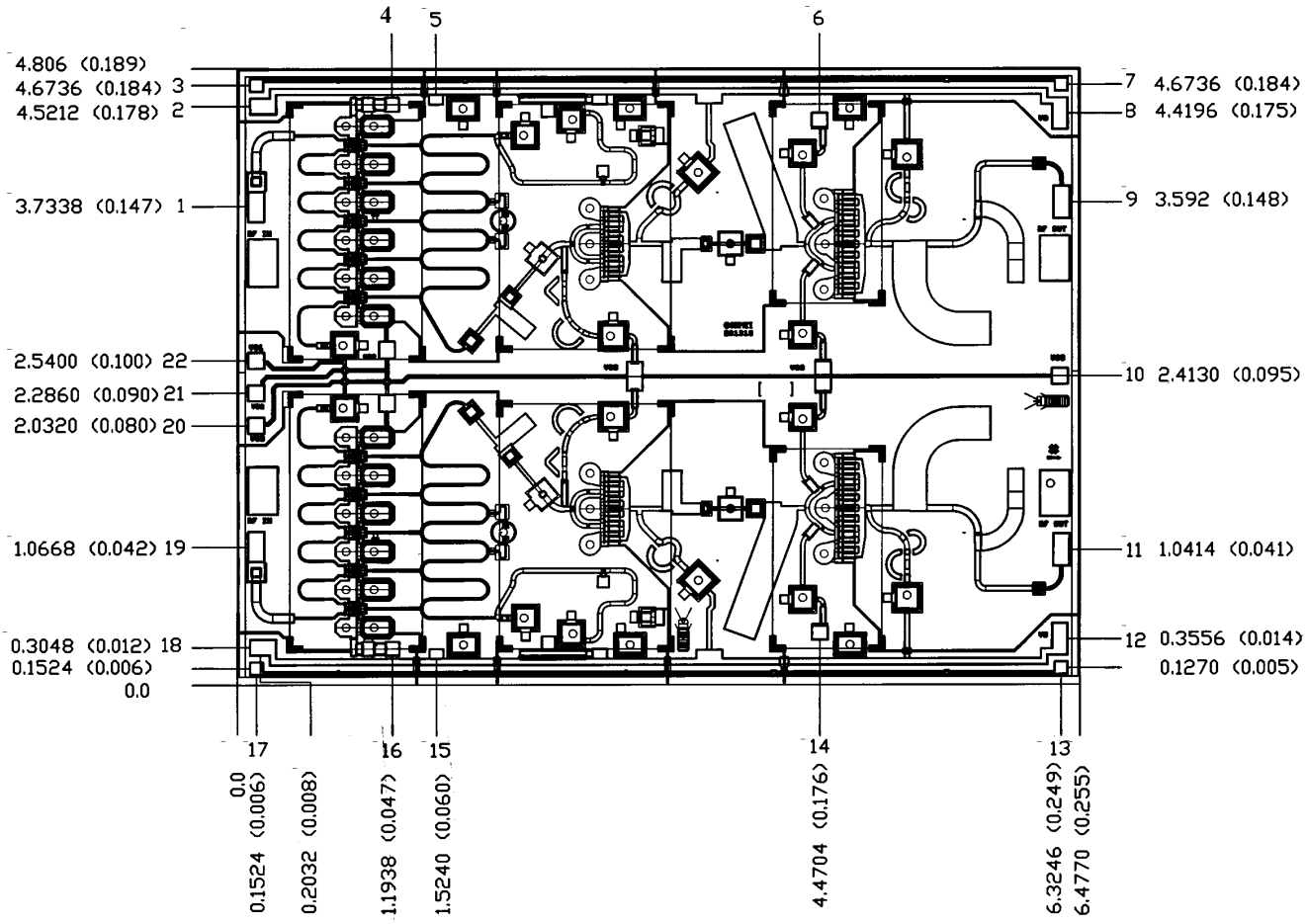
Refer to TriQuint's Recommended Assembly Instructions for GaAs Products.

SINGLE CHANNEL
ASSEMBLY DIAGRAM



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

MECHANICAL DRAWING



Units: millimeters (inches)
Thickness: 0.1016 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.0508 (0.002)

Bond pad #1, 19 (RF Input)	0.1270 x 0.2311 (0.0050 x 0.0091)
Bond pad #2, 18 (Vd)	0.1981 x 0.1219 (0.0078 x 0.0048)
Bond pad #3, 7, 13, 17:	0.0965 x 0.0965 (0.0039 x 0.0039)
Bond pad #4, 16	0.1143 x 0.1143 (0.0045 x 0.0045)
Bond pad #5, 15:	0.0991 x 0.0737 (0.0039 x 0.0029)
Bond pad #6, 10, 14, 21, 22, 23:	0.1270 x 0.1270 (0.0050 x 0.0050)
Bond pad #8, 12:	0.1168 x 0.2438 (0.0046 x 0.0096)
Bond pad #9, 11 (RF Output):	0.1321 x 0.2616 (0.0052 x 0.0103)

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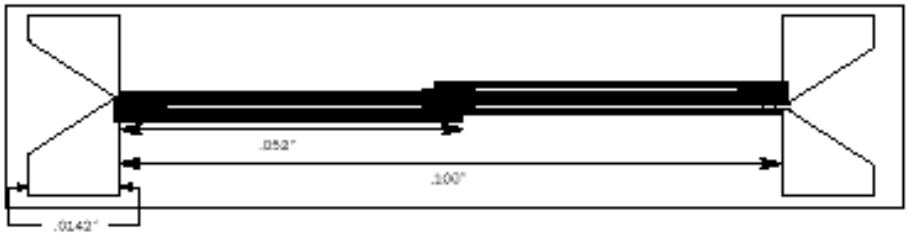
Application Notes: **Balanced Configuration Utilizing Lange Couplers**

INTRODUCTION

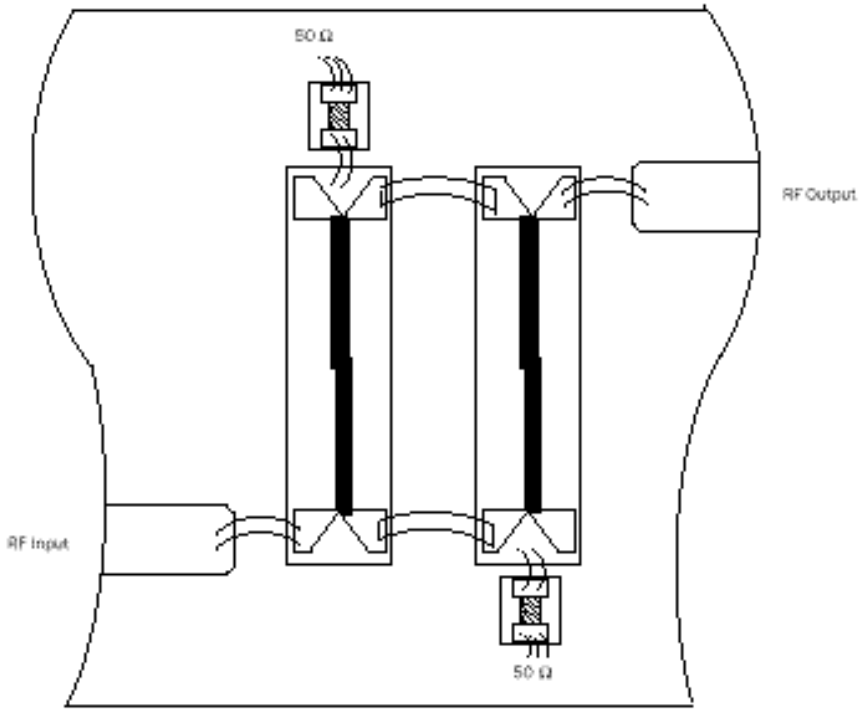
This section describes the operation of the TGA6316 in a balanced amplifier configuration utilizing Lange Couplers. Bias for V_{G2} is derived from an optional on-chip voltage divider. Bonding pads 4 and 5 together using a 1-mil bond wire provides 1.5 V to V_{G2} with 8 V applied to the drain. The typical output power at 3-dB gain compression for the balanced configuration is 31-dBm at mid-band. A performance comparison between the single-ended and balanced configurations is shown in the Typical Output Power on the next page. The Lange Coupler Layout shown below utilizes 15-mil-thick alumina as the substrate material.

LANGE COUPLER LAYOUT

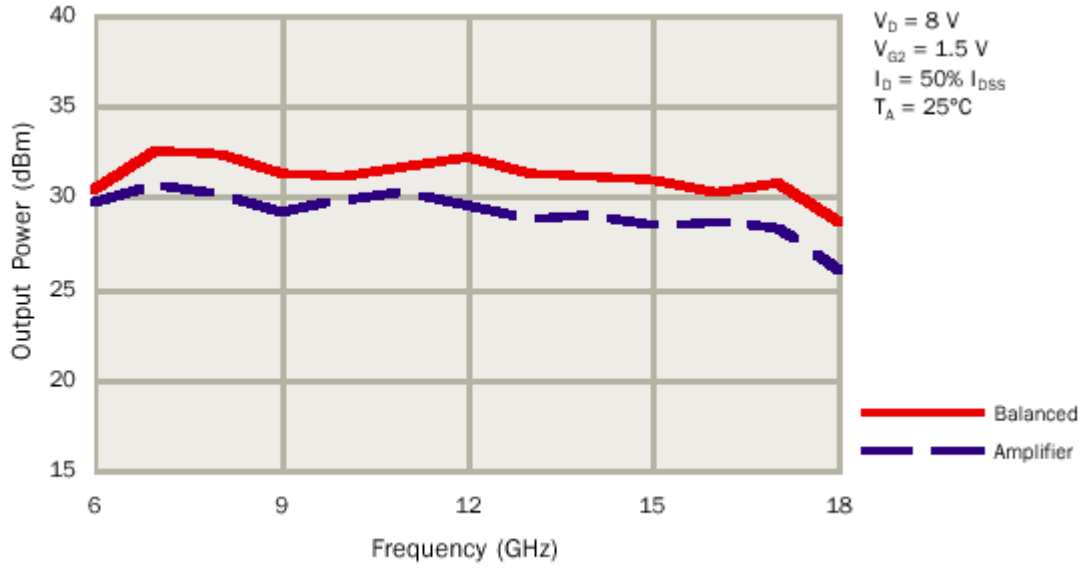


Lange coupled lines: W = .0011", S= .0009".
15-mil Alumina Substrate

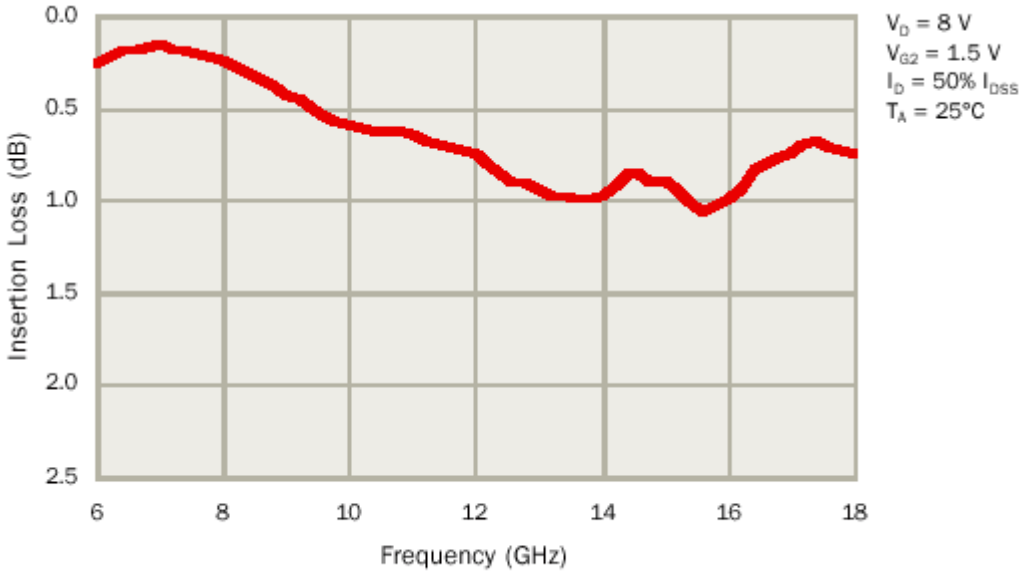
TWO LANGE COUPLERS CASCADE ASSEMBLY DIAGRAM



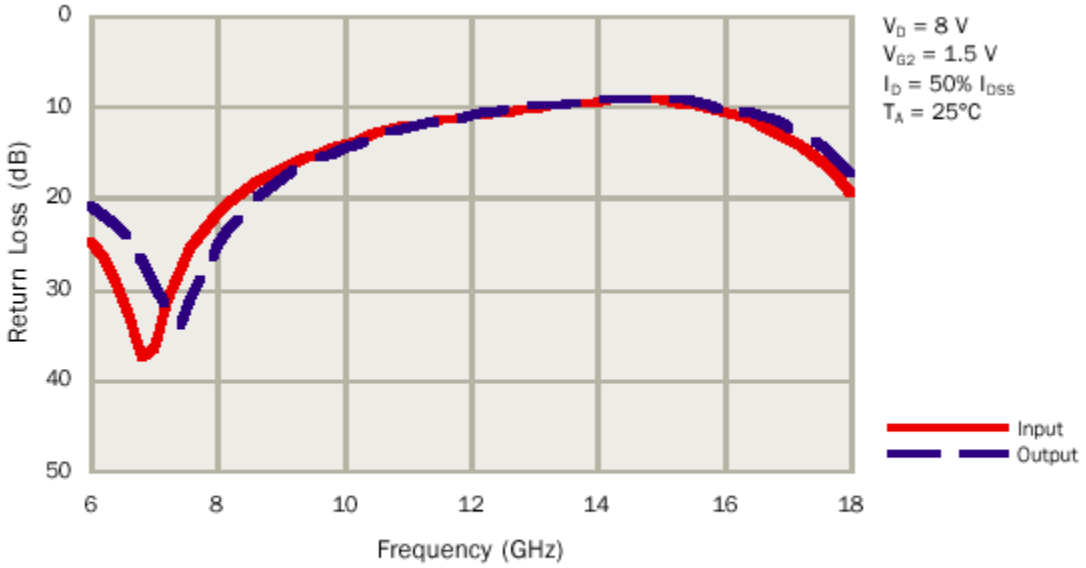
TYPICAL OUTPUT POWER P3dB



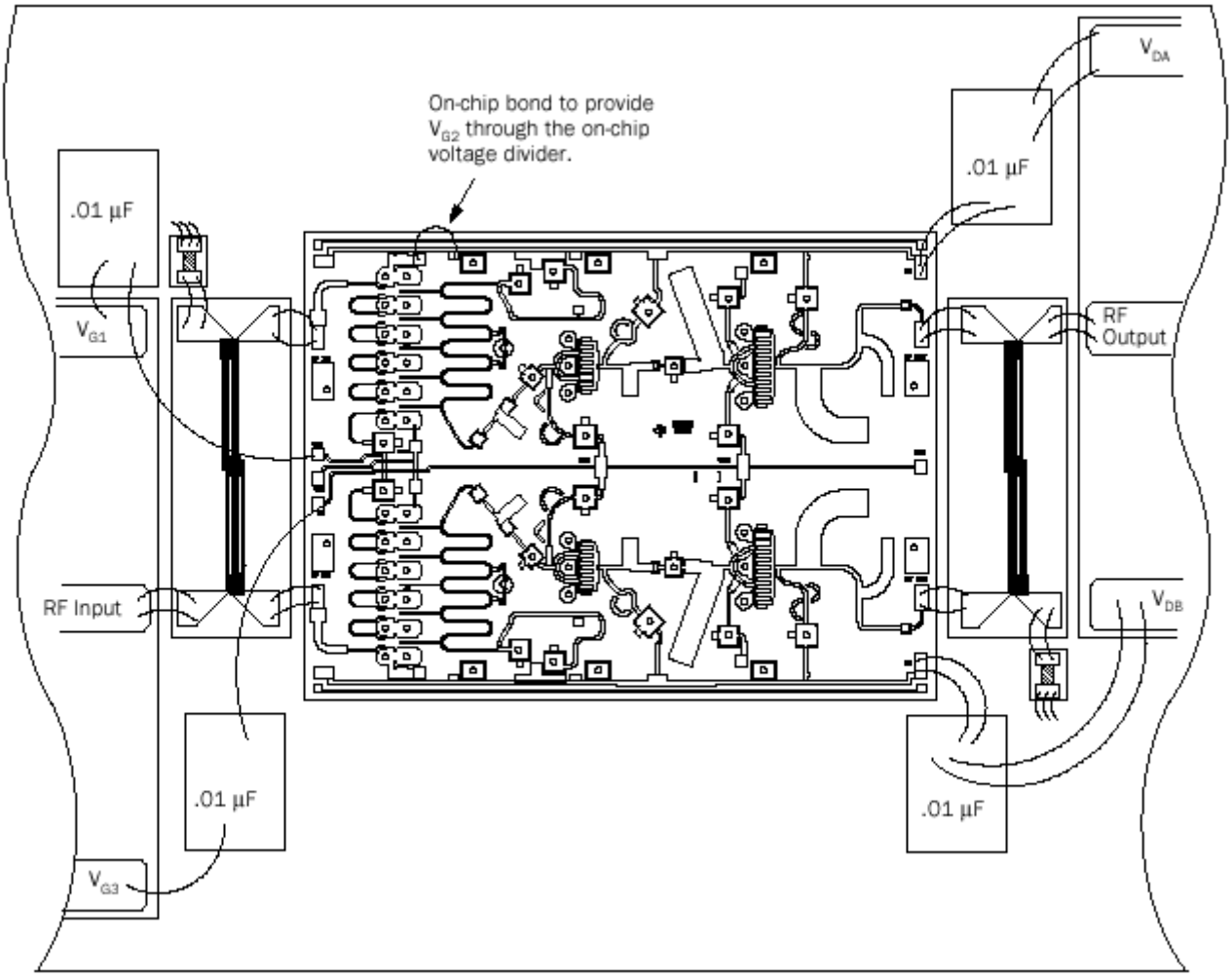
TYPICAL INSERTION LOSS FOR TWO LANGE COUPLERS



TYPICAL RETURN LOSS FOR LANGE COUPLERS



RECOMMENDED ASSEMBLY DIAGRAM FOR BALANCED CONFIGURATION



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